LMN7002KTFF 60V N-Channel Enhancement Mode MOSFET

Features

- 60V/0.5A, $R_{DS(ON)}$ =3.0Ω@V_{GS} = 10V
- 60V/0.4A, $R_{DS(ON)}$ =4.0Ω@V_{GS} = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- ESD Protection (2KV) Diode design-in
- DFN1006-3L package design

Product Description

LMN7002K, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

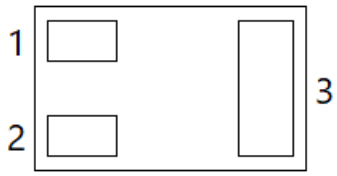
These devices are particularly suited for low voltage power management, such as smart phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

Applications

- Drivers:Relays,Solenoids,Lamps,Hammers, Display, Memories, Transistors, etc.
- High saturation current capability.
  Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

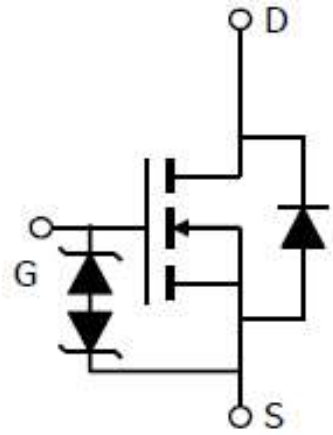
Pin Configuration

LMN7002KTFF (DFN1006-3L)



Transparent Top Views

Pin	Description
1	Gate
2	Source
3	Drain



Ordering Information

Part Number	P/N	PKG Code	Pb Free Code	Package	Quantity Reel
LMN7002KTFF	LMN7002K	TF	F	DFN1006-3L	10000 pcs

Marking Information

Part Marking	Part Number	LFC code
e WMM	**e**	WMM

Absolute Maximum Ratings

(T_A=25ºC Unless otherwise noted)

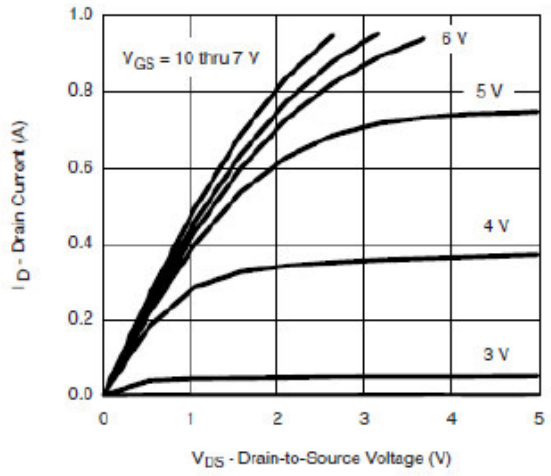
Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A=25ºC	0.27	A
		T_A=70ºC	0.21	
I_{DM}	Pulsed Drain Current		0.90	A
P_D	Power Dissipation	T_A=25ºC	0.35	W
		T_A=70ºC	0.22	
T_J	Operating Junction Temperature Range		-55 to +150	ºC
T_{STG}	Storage Temperature Range		-55 to +150	ºC
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		357	ºC/W

Electrical Characteristics

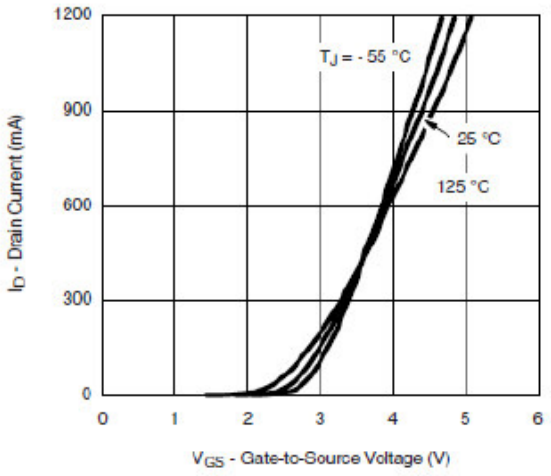
(T_A=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1.0		2.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			10	uA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=48V, V_{GS}=0V			1	uA
		V_{DS}=48V, V_{GS}=0V, T_J=85ºC			30	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=0.5A		1.9	3.0	Ω
		V_{GS}=4.5V, I_D=0.4A		2.4	4.0	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=0.2A		0.5		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=0.5A		0.7	1.3	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		30		pF
C_{oss}	Output Capacitance			8		
C_{rss}	Reverse Transfer Capacitance			5		
Q_g	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=0.25A		500		pC
Q_{gs}	Gate-Source Charge			100		
Q_{gd}	Gate-Drain Charge			150		
$t_{d(on)}$	Turn-On Time	V_{DD}=30V, I_D=0.2A, V_{GS}=4.5V, R_L = 150Ω, R_G=10Ω		10	20	ns
T_r				35	50	
$t_{d(off)}$	Turn-Off Time			20	30	
T_f				40	60	

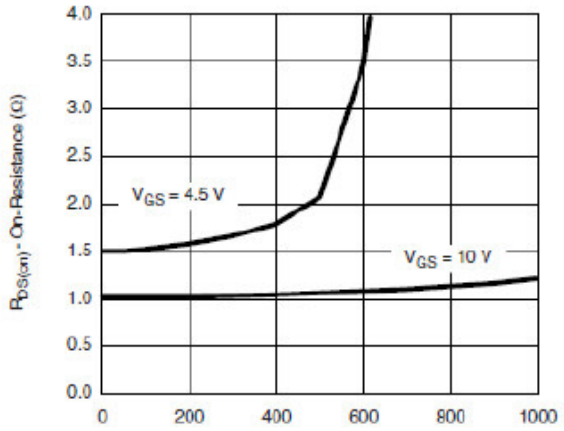
Typical Performance Characteristics



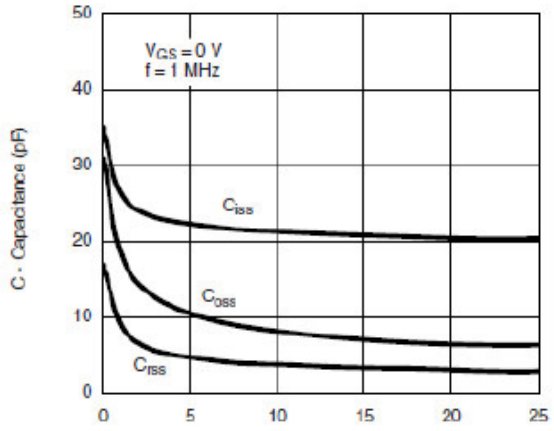
Output Characteristics



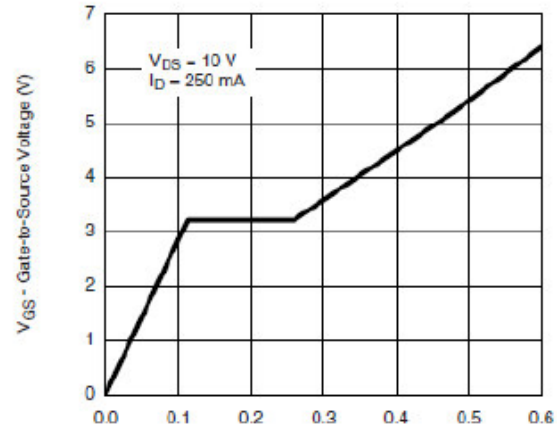
Transfer Characteristics



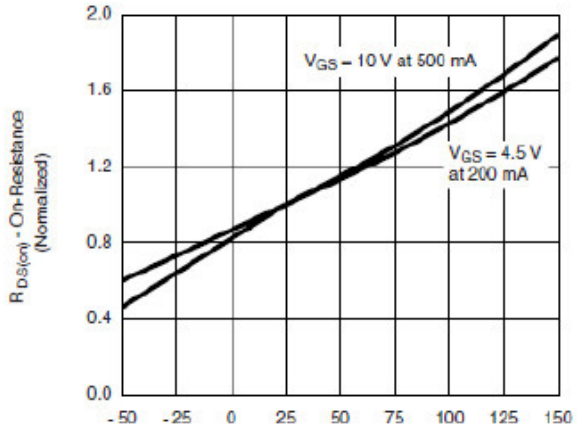
On-Resistance vs. Drain Current



Capacitance

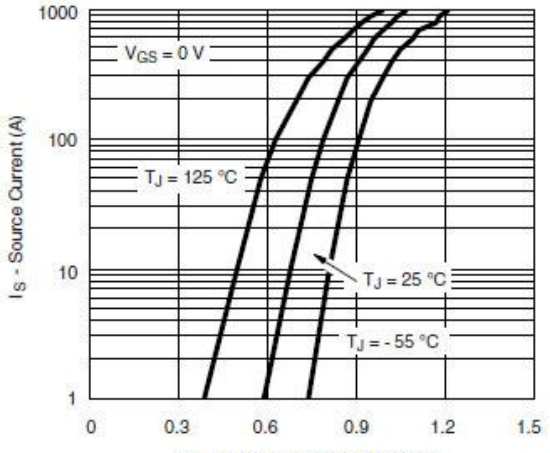


Gate Charge

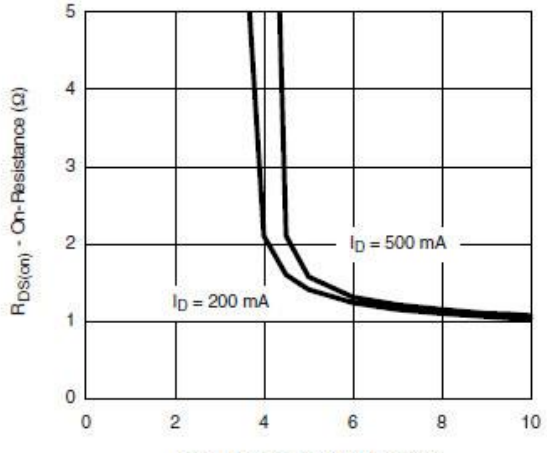


On-Resistance vs. Junction Temperature

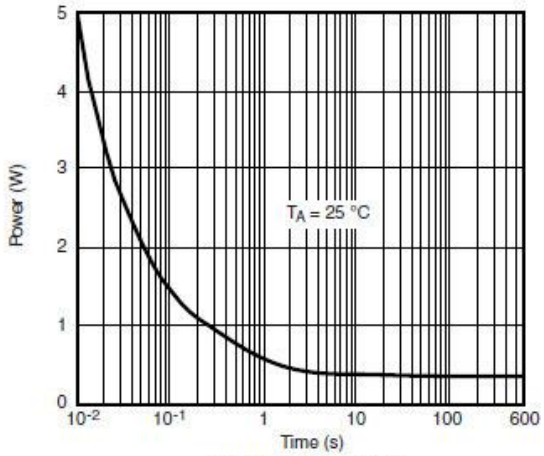
Typical Performance Characteristics (continue.)



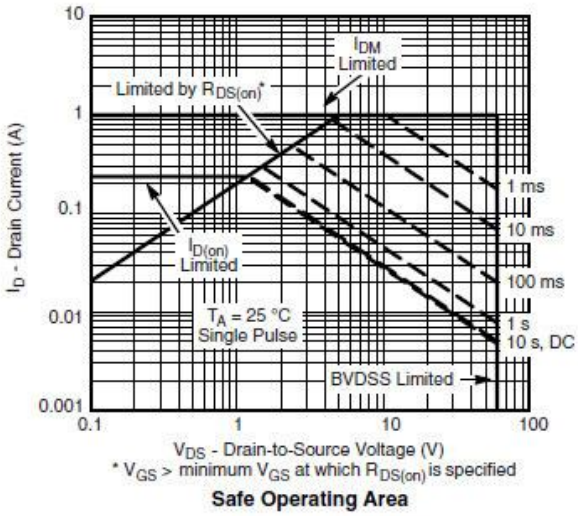
Source-Drain Diode Forward Voltage



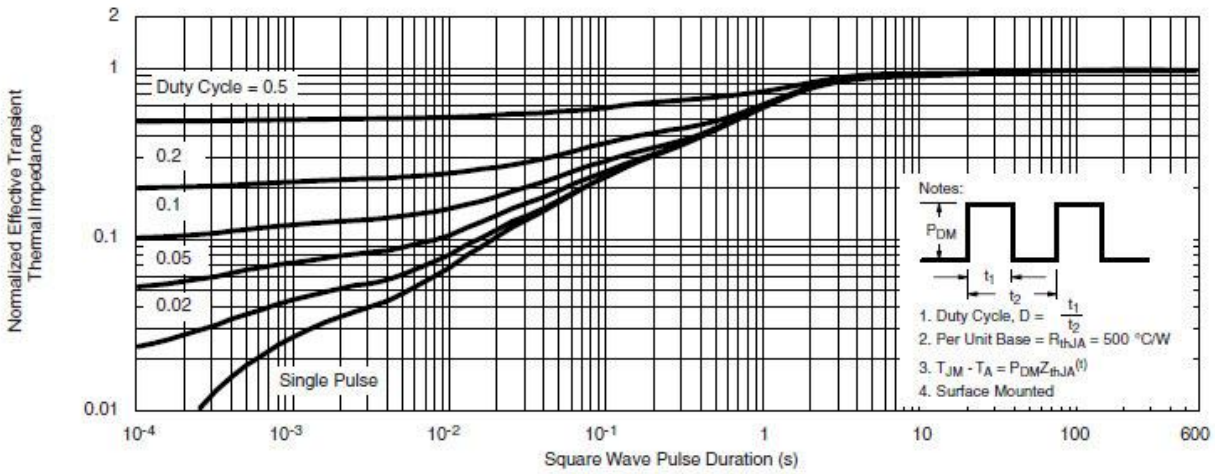
On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power



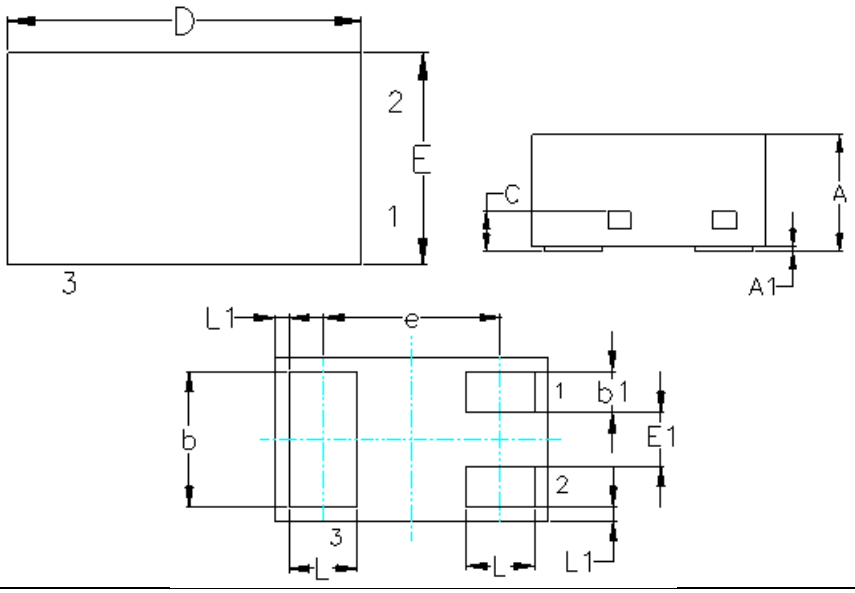
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

Package Dimension

DFN1006-3L



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
b	0.450	0.550	0.018	0.022
b1	0.100	0.200	0.004	0.008
C	0.120	0.180	0.005	0.007
D	0.950	1.050	0.037	0.041
E	0.550	0.650	0.022	0.026
E1	0.150	0.250	0.006	0.010
e	0.650 BSC		0.026 BSC	
L	0.200	0.300	0.008	0.012
L1	0.050 REF		0.002 REF	