LMN3136P 30V N-Channel MOSFETs

Features

- 30V, 5.3A, $R_{DS(ON)}$=36mΩ@V_{GS}=4.5V
- Improved dv/dt capability
- Fast switching
- Suit for 2.5V Gate Drive Applications
- Green Device Available
- SOT-23 package design

Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

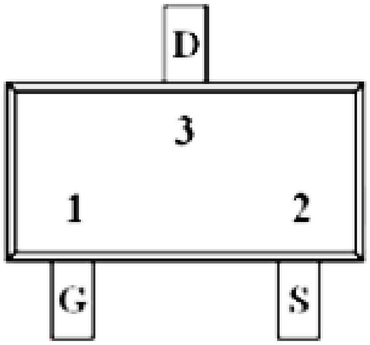
These devices are well suited for high efficiency fast switching applications.

Applications

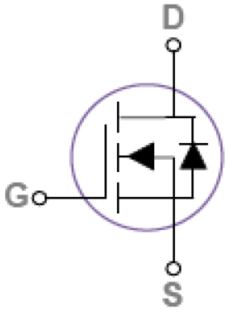
- Notebook
- Load Switch
- LCD applications

Pin Configuration

LMN3136PJZF (SOT-23)



PIN	Description
1	Gate
2	Source
3	Drain



Ordering Information

LMN3136P	JZ	F
LFC P/N	PKG code	Pb Free code

Marking Information

P	XWMM
Part Number	LFC code

Part Number	Package	Part Marking	Quantity
LMN3136PJZF	SOT-23	XWMM	3000pcs

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current	TC=25℃	5.3	A
		TC=100℃	3.4	
I_{DM}	Pulsed Drain Current[1]		21.2	A
P_D	Power Dissipation (Tc=25℃)		1.56	W
	Power Dissipation (Derate above 25℃)		0.012	W/℃
T_J	Operating Junction Temperature Range		-50 to +150	℃
T_{STG}	Storage Temperature Range		-50 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		80	℃/W

Electrical Characteristics

(T_A=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Static				
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30			V
△BV_{DSS}/△T_J	BV_{DSS} Temperature Coefficient	Reference to 25℃, I_D=1mA		0.06		V/℃
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.4	0.6	0.9	V
△$V_{GS\ (th)}$	$V_{GS(th)}$ Temperature Coefficient			-3		mV/℃
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	uA
		V_{DS}=24V, V_{GS}=0V, T_A=125ºC			10	
I_S	Continuous Source Current	V_G=V_D=0V, Force Current			5.3	A
I_{SM}	Pulsed Source Current				21.2	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-10.0V, I_D=4A		31	36	mΩ
		V_{GS}=2.5V, I_D=3A		36	45	
g_{FS}	Forward Transconductance	V_{DS}=10V, I_D=3A		7		S
V_{SD}	Diode Forward Voltage	I_S=1.0A, V_{GS}=0V			1	V
		Dynamic				
Q_g	Total Gate Charge^{2,3}	V_{DS}=10V, V_{GS}=4.5V, I_D=4A		8.4	12	nC
Q_{gs}	Gate-Source Charge^{2,3}			1	2	
Q_{gd}	Gate-Drain Charge^{2,3}			2.2	4	
C_{iss}	Input Capacitance	V_{DS}=10V, V_{GS}=0V, f=1MHz		695	1000	pF
C_{oss}	Output Capacitance			45	65	
C_{rss}	Reverse Transfer Capacitance			36	50	
$t_{d(on)}$	Turn-On Time^{2,3}	V_{DD}=10V, I_D=1A, V_{GS}=4.5V, R_G=25Ω		4.5	9	ns
t_r				13	25	
$t_{d(off)}$	Turn-Off Time^{2,3}			27	51	
t_f				8.3	16	
R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.5	3	Ω

Note:

1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

Typical Performance Characteristics

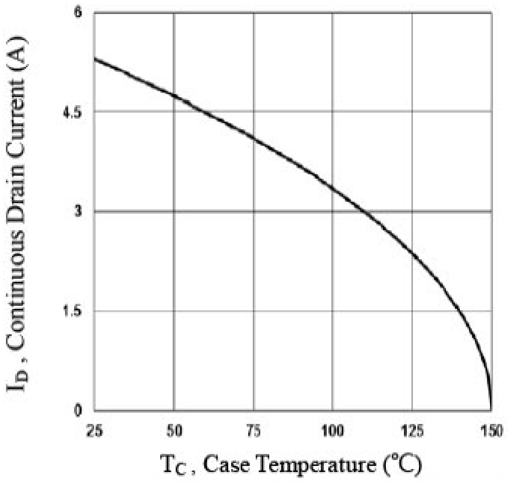


Fig.1 Continuous Drain Current vs. T_c

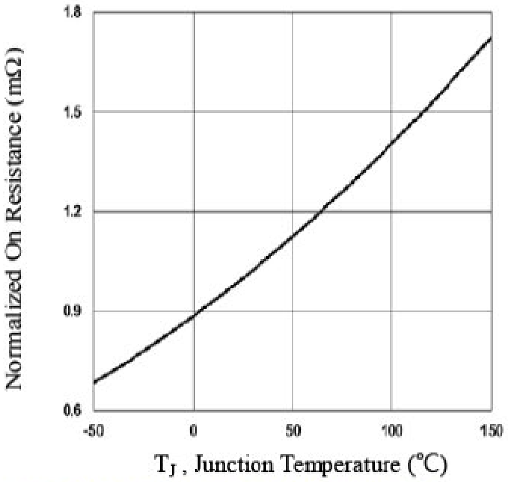


Fig.2 Normalized RDSON vs. T_J

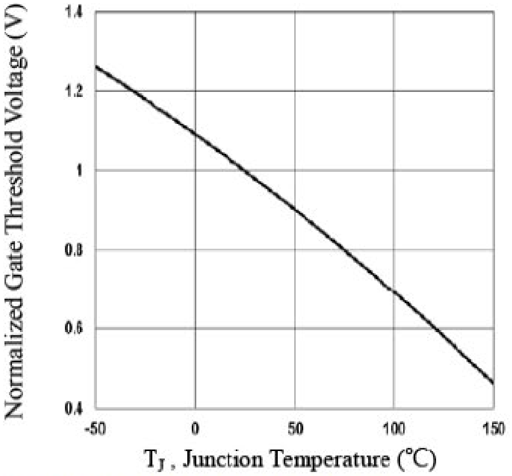


Fig.3 Normalized V_{th} vs. T_J

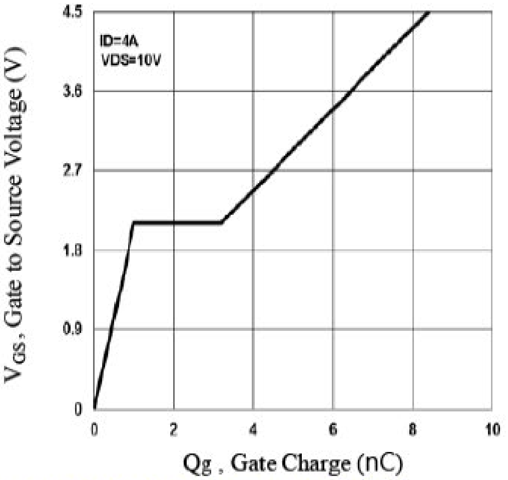


Fig.4 Gate Charge Waveform

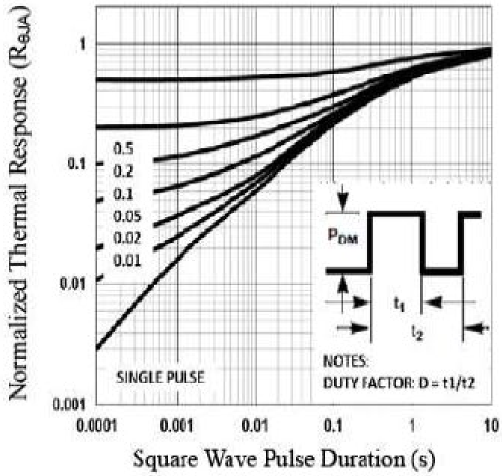


Fig.5 Normalized Transient Impedance

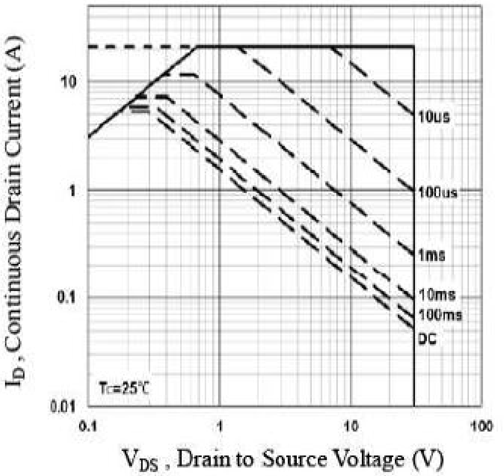
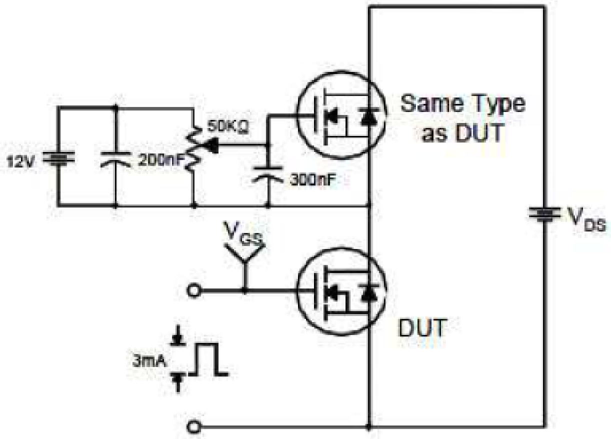
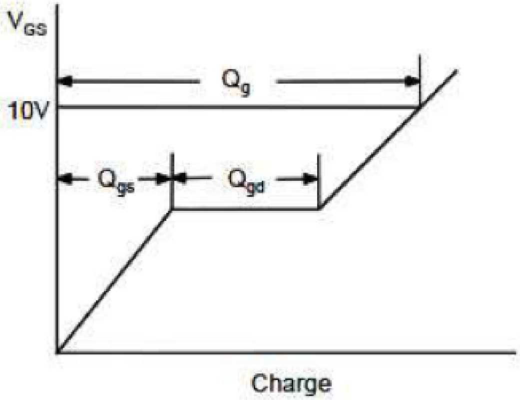


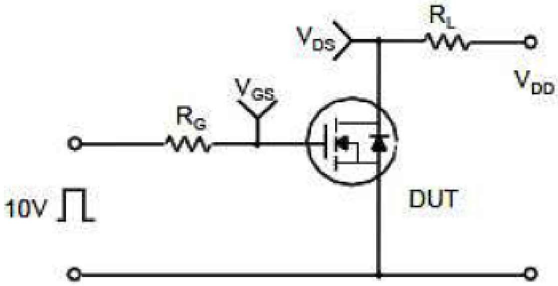
Fig.6 Maximum Safe Operation Area

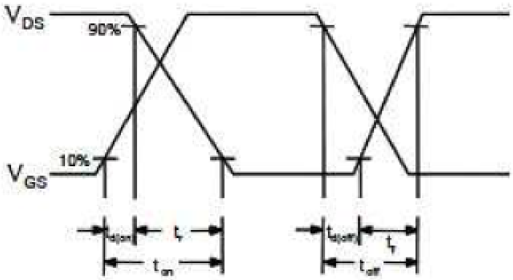
Gate Charge Test Circuit & Waveform



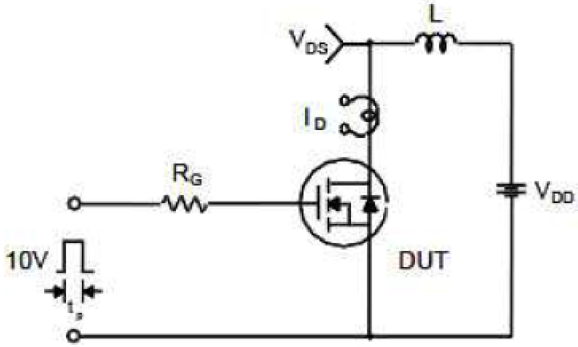


Resistive Switching Test Circuit & Waveforms

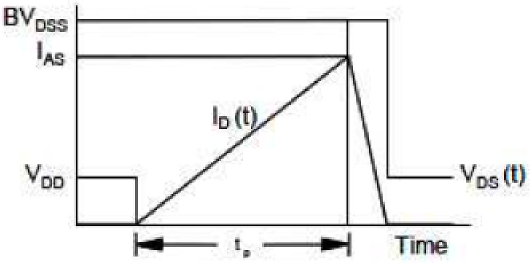




Unclamped Inductive Switching Test Circuit & Waveforms

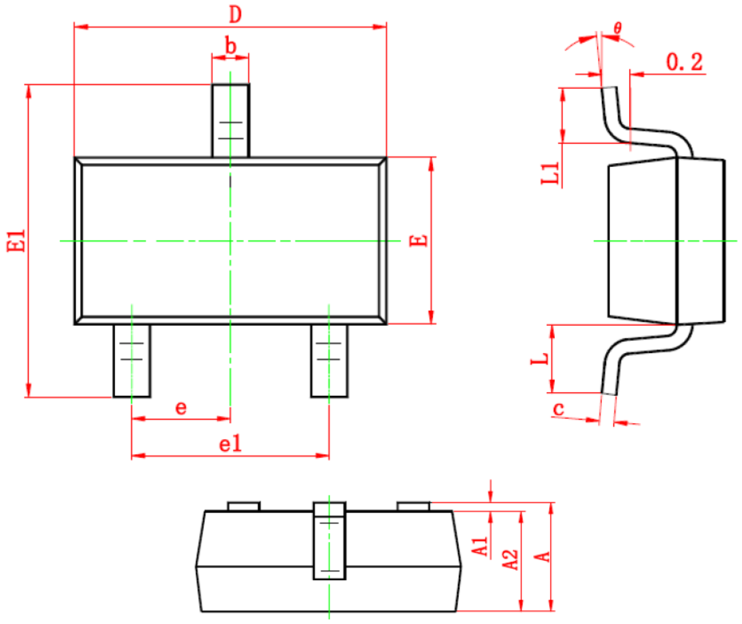


$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Package Dimension:

SOT-23



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550REF		0.022REF	
L1	0.300	0.500	0.012	0.020
θ	0º	8º	0º	6º

NOTICE: