40V Synchronous CC/CV Buck Controller

Features

- Wide Input Voltage from 4.5V to 40V
- Adjustable Switching Frequency
- High Efficiency
- High Duty-Cycle Up to 99%
- Programmable External Soft-Start
- CC/CV Control
- Auto Recovery after Faults
- Low Output Short Current
- Programmable Over Current Setting
- Input Over-Voltage Protection
- Over-Temperature Protection
- Thermal Enhanced TSSOP-14 Package
- RoHS Compliant

Product Description

The LPD6572 is a synchronous buck controller capable of regulating the output voltage below the input voltage. The LPD6572 operates over a wide input voltage range of 4.5V to 40V to support a variety of applications.

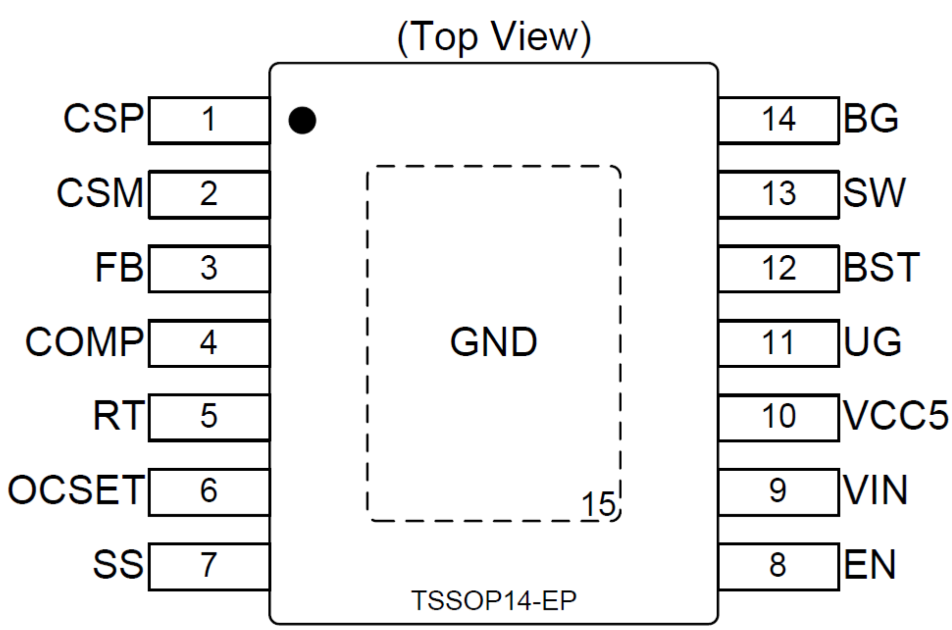
The LPD6572 employs voltage-mode control for superior load and line regulation. The switching frequency is programmed by an external resistor. This device also features a programmable soft-start function and offers protection features including cycle-by-cycle current limiting, input undervoltage lockout (UVLO) and thermal shutdown.

The LPD6572 is available in a TSSOP14-EP package, provides a very compact system solution and good thermal conductance.

Applications

- Car Charger
- Rechargeable Portable Devices
- USB Power Delivery
- Automotive Industry

Pin Configuration



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Ordering Information

Part Number	Package	Shipment
LPD6572-ATD	TSSOP14-EP	Tape & Reel / 2500

***A: Output Voltage Adjustable**
***TD: TSSOP14-EP**

Simplified Application Circuit:

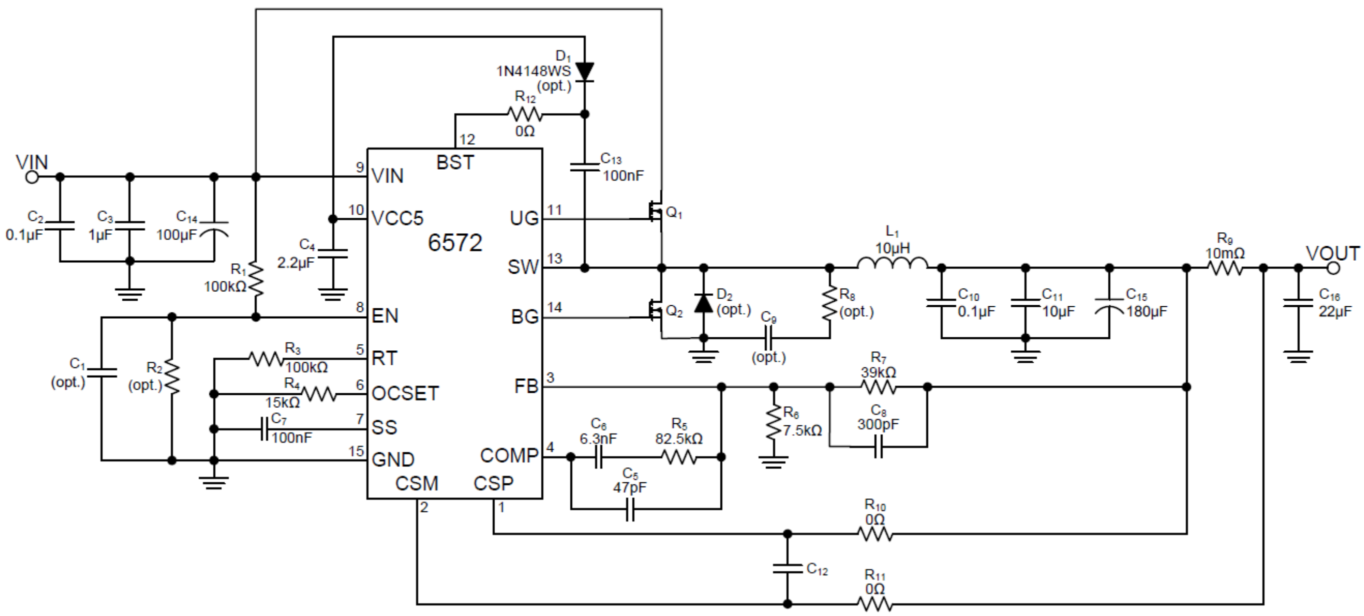


Figure 1 Simplified Application Circuit

Pin Function Description:

Pin NO.	Pin Name	Pin Description
1	CSP	Positive input pin for output load current sensing.
2	CSM	Negative input pin for output load current sensing.
3	FB	Voltage Feedback Input Pin. Connecting FB and VOUT with a resistive voltage divider. This IC senses feedback voltage via FB and regulate it at 0.808V.
4	COMP	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to FB pin.
5	RT	Switching frequency programming pin. An external resistor is connected to the RT pin and GND to set the switching frequency.
6	OCSET	Valley current limit programming pin. An external resistor is connected to the OCSET pin and GND to set the valley current limit.
7	SS	Soft-start programming pin. A capacitor between the SS pin and GND programs soft-start time.
8	EN	Enable Input Pin. This pin provides a digital control to turn the controller on/off.
9	VIN	Power Supply Input Pin. Drive 4.75V to 40V voltage to this pin to power on this chip. Connecting a 10uF ceramic bypass capacitor between VIN and GND to eliminate noise.
10	VCC5	BG Driver Bias Supply. Decouple with a 2.2uF capacitor.
11	UG	Output of the high-side gate driver. Connect to the gate of the high-side MOSFET.
12	BST	High Side Gate Drive Boost Input. A 100nF capacitor is recommended to connect from this pin to SW. It can boost the gate drive to fully turn on the external high-side MOSFET.
13	SW	Power Switching Output. It is the output pin that internal high side NMOS switching to supply power.
14	BG	Output of the low-side gate driver. Connect to the gate of the low-side MOSFET.
15	GND	Exposed Pad. Ground Pin.

Absolute Maximum Ratings (1)

Input Supply Voltage VIN .... -0.3V ~ 42V
EN, CSP, CSM Voltage V_{EN}, V_{CSP}, V_{CSM} .... -0.3V ~ 42V
SW Voltage V_{SW} .... -0.3V (-5V for < 10ns) ~ 42V (46V for < 5ns)
Boost Voltage V_{BST} .... -0.3 ~ (V_{SW} + 6V)
UG Voltage V_{UG} .... V_{SW} ~ (V_{SW} + 6V)
All Other Pins Voltage .... -0.3V ~ 6V
Maximum Junction Temperature .... 150°C
Storage Temperature .... -55°C ~ 150°C
Lead Temperature (Soldering 10 sec) .... 260°C
ESD Classification (HBM) .... Class 2
Power Dissipation (PD) @ TA = 25°C 2.5W

Recommended Operating Conditions (2)

Input Supply Voltage V_{IN} .... 5V ~ 40V
Ambient Temperature TA .... -40°C ~ 85°C

Recommended Operating Conditions (2)

TSSOP-14(Exposed Pad), θ_{JA} .... 40°C/W
TSSOP-14(Exposed Pad), θ_{JC} .... 7.5°C/W

Notes:
(1). Stresses exceed those ratings may damage the device.
(2). If out of its operation conditions, the device is not guaranteed to function.

Electrical Characteristics

(VIN = 12V, TA = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} Input Supply Voltage			4.5		40	V
Quiescent Current (non-switching)	I_Q	V_{FB}=0.85V		1.5	2	mA
Standby Supply Current (no loading)					20	mA
Regulation Voltage	V_{CC5}		4.5	5.25		V
Feedback Reference Voltage	V_{FB}	4.5V≦V_{IN}≦40V	792	808	824	mV
Error Amplifier Transconductance	G_{EA}	Δ I_{COMP} = ±10μA		850		μA/V
Switching frequency	F_{SW}	RT=100kΩ	200	250	300	kHz
Maximum Duty Cycle	DMAX	V_{FB} = 0.7V	97	98	99	%
Minimum On Time	TON			250		ns
Average Current Loop Regulation	V_{SNS}	V_{SNS}=V_{CSP}-V_{CSM}		50		mV
Input UVLO Threshold		VIN Rising		4.2	4.4	V
Input UVLO Threshold Hysteresis				600		mV
Soft-Start Pull Up Current	I_{SS}	V_{SS}=0		6		μA
SS Clamp Voltage	$V_{SS(CLP)}$	SS Open		1.46		V
Thermal Shutdown Threshold (3)				160		℃
Gate Driver Sink Impedance (3)	R_{Sink}			0.9		Ω
Gate Driver Source Impedance (3)	R_{Source}			3.3		Ω

Notes:
(3) Guaranteed by design.

Functional Block Diagram

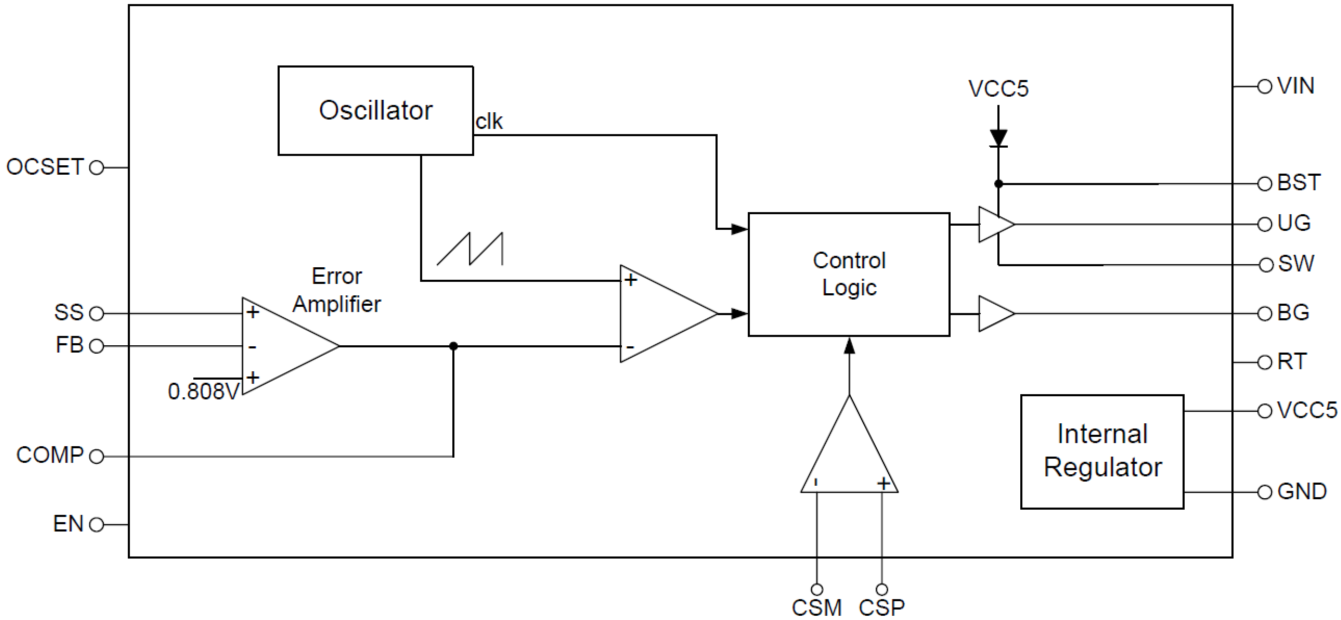


Figure2 BLOCK DIAGRAM

PCB Layout Guideline

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show bellow:

1. Keep the traces of the main current paths as short and wide as possible to minimize parasitic inductance and resistance.
2. Place VIN bypass capacitor (CIN) close to the device pins (VIN and GND). The loop area formed by CIN and VIN/GND pins must be minimized.
3. Minimize the switching loop area formed by VIN, SW and the power MOSFETs of UG and BG.
4. Use a combination of bulk capacitors and smaller ceramic capacitors with low series impedance for the input and output capacitors. Place the smaller capacitors closer to the IC.
5. Place feedback resistors close to the FB pin. Connect feedback network behind the output capacitors.
6. Place compensation components close to the COMP pin.
7. Place the BST bootstrap capacitor close to the IC and connect directly to the BST to SW pins.
8. Keep the sensitive signal (FB, COMP, CSP, CSM, RT, OCSET and SS) away from the switching signal (BST, SW, UG, BG).
9. Use Kelvin connections to sense resistor for the current sense signals CSP and CSM.
10. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacities.
11. Place the VCC5 bypass capacitor close to the controller IC, between the VCC5 and GND pins.
12. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the

exposed pad should be maximized to improve thermal performance.

13. Multi-layer PCB design is recommended.

Application Circuit

Fix 5V Output Voltage

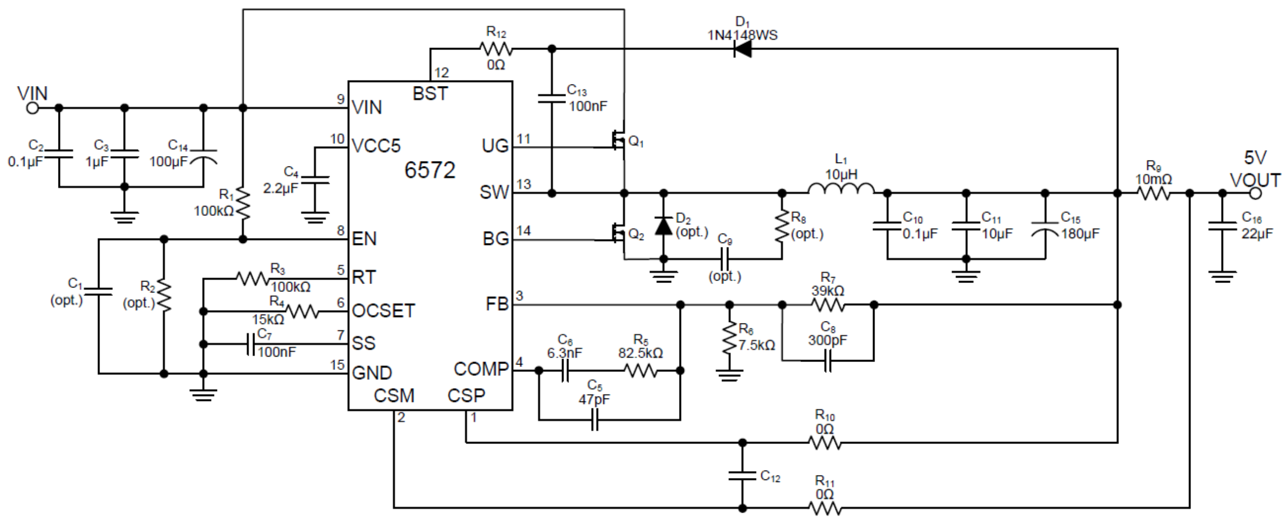


Figure 3 For 5V Output Voltage Application Circuit

Input Voltage < 5.5V

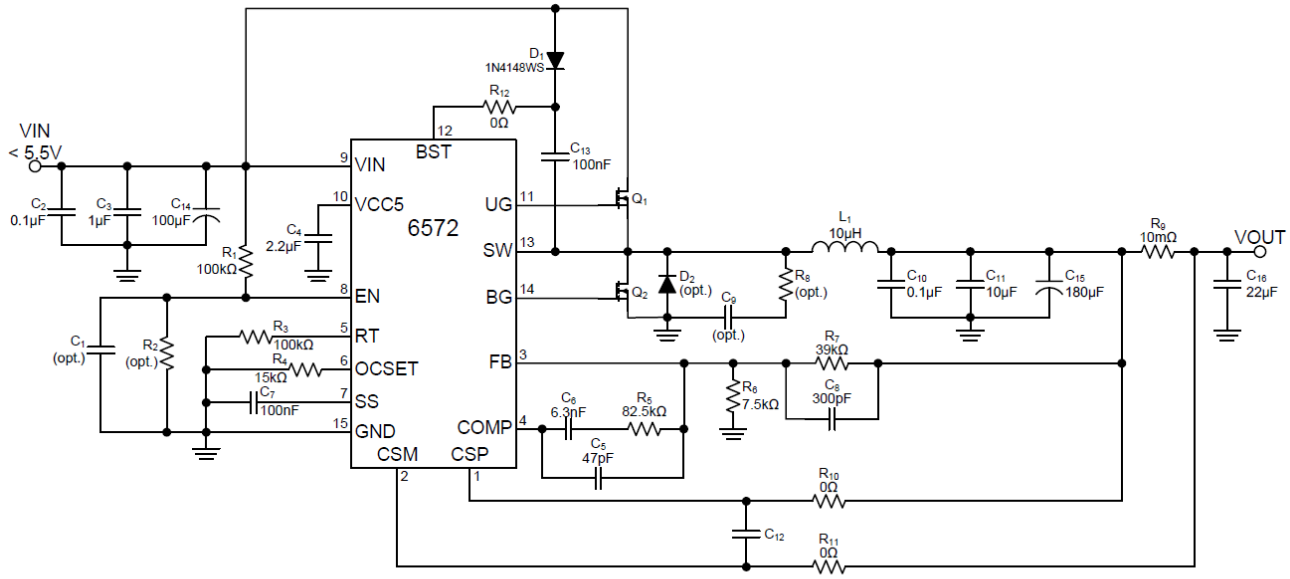
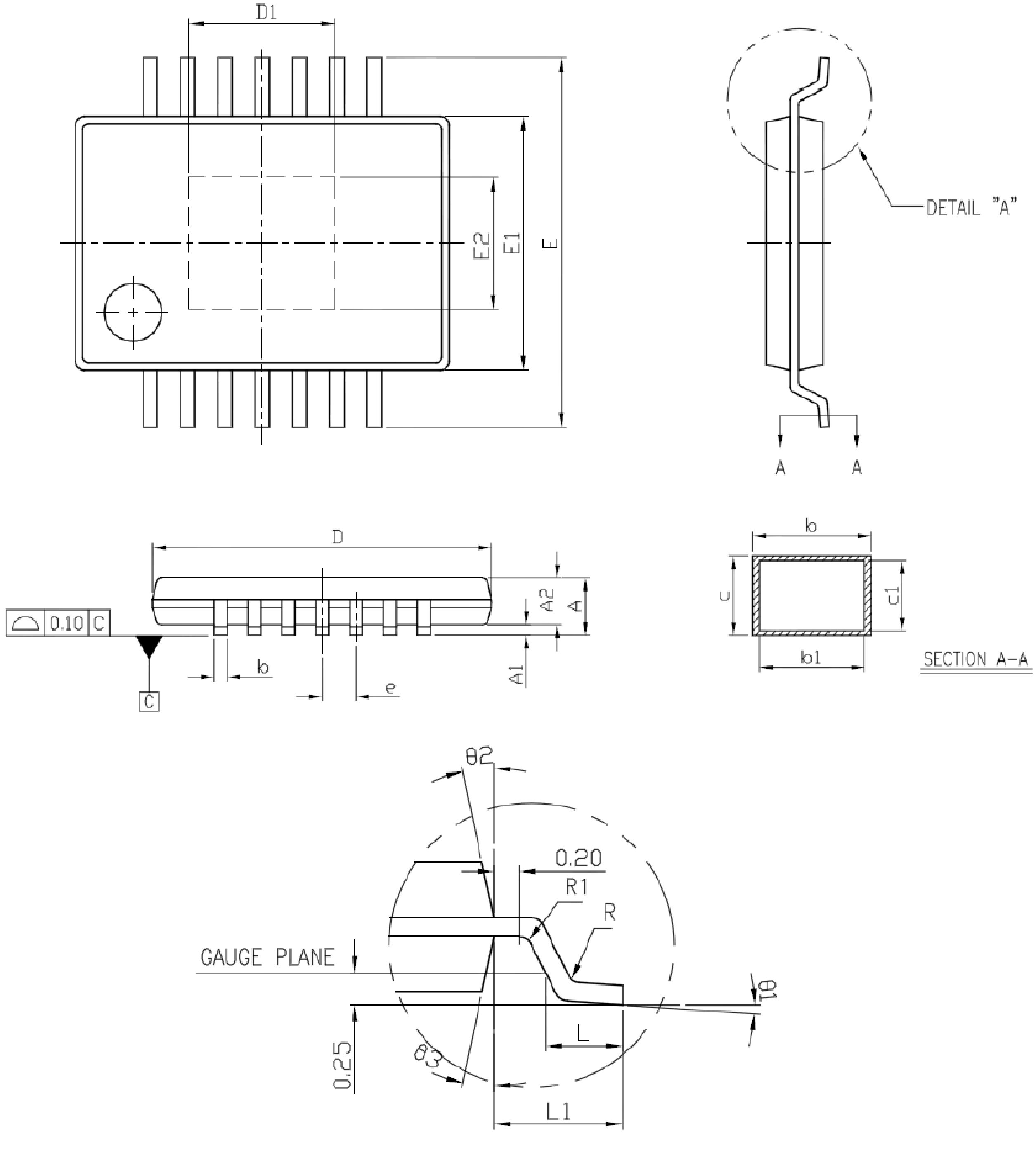


Figure 4 For VIN < 5.5V Application Circuit

Package Information

TSSOP14-EP



DETAIL A

Symbols	Dimensions in Millimeters			Dimensions in Inches		
	Min.	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	-----	-----	1.2	-----	-----	0.047
A1	0.05	-----	0.15	0.002	-----	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
L	0.45	0.60	0.75	0.018	0.024	0.030
E		6.40			0.2852	
E1	4.30	4.40	4.50	0.169	0.173	0.177
R	0.09	-----	-----	0.004	-----	-----
R1	0.09	-----	-----	0.004	-----	-----
b	0.19	-----	0.30	0.007	-----	0.012
b1	0.19	0.22	0.25	0.007	0.009	0.010
c	0.09	-----	0.20	0.004	-----	0.008
c1	0.09	-----	0.16	0.004	-----	0.006
L1		1.0			0.039	
e		0.65			0.026	
θ1	0	-----	8°	0	-----	8°
θ2		12°			12°	
θ3		12°			12°	
D	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.92	-----	2.54	0.076	-----	0.100
E2	1.67	-----	2.29	0.066	-----	0.090