# 18.5V, 4 Rail Power Management IC with Safety Monitoring for Camera Modules AEC-Q100 Qualified

## DESCRIPTION

The LPC710 is a complete power management solution, which integrates three high efficiency step-down DC/DC converters, and high-PSRR LDO, and flexible logic interface.

The Buck1 step-down converter has an input voltage range up to 18.5V for the power over Coax(PoC). All step down converters operate in a forced fixed-frequency PWM mode. 2.2MHz or 3.3MHz selectable switching frequency during CCM mode greatly reduces external inductor and capacitor value. Full protection features include UVLO, OCP, OVP and thermal shutdown.

The LPC710 requires a minimal number of external components, and is available in space-saving 16-pin QFN (3mmx3mm).

## Features

- AEC-Q100 Grade 1
- ASIL-B compliant
- FMEA Compliant Pin Placement and Protection Mechanisms
- Three Step-Down Converters (HVBuck1, LVBuck2 and LVBuck3)
  - Peak Current Mode PWM Operation
  - Selectable Switching Frequency at 2.2MHz or 3.3MHz
  - Stepped Triangle Spread Spectrum with on/off Function
  - HVBuck1 Input Voltage from 4V to 18.5V, Adjustable Output Voltage and Up to 2A Output Current
  - LVBuck2 Input Voltage from 2.7V to 5V, Fixed Output Voltage and 1.5A Output Current
  - LVBuck3 Input Voltage from 2.7V to 5V, Fixed Output Voltage and 750mA Output Current
- Low Dropout Regulator (LDO)
  - Input Voltage from 2.7V to 5V and 300mA Output Current
  - 10 Adjustable Output Voltage Settings via RSET Pin
  - High PSRR : 60dB at 100kHz, 55dB at 2MHz
  - Pins Related to LVBuck2/LVBuck3 Allowable Floating if Channel Unused
- Output Function
  - Sequence Control for External resistor
  - Power Status Indication via PG
- 6 Flexible Power Sequence Settings via SEQ Pin
- Small Form Factor QFN-16L 3x3

## APPLICATIONS

- Automotive Camera Modules
  - Surround View Camera
  - Front View Camera
  - Rear View Camera
  - Driver Monitoring System
  - Cabin Monitor
  - Dash Cam DVR
  - eMirror
- Automotive Sensor Applications
- Automotive Secondary Regulation
- Space Constrained Applications

## TYPICAL APPLICATION

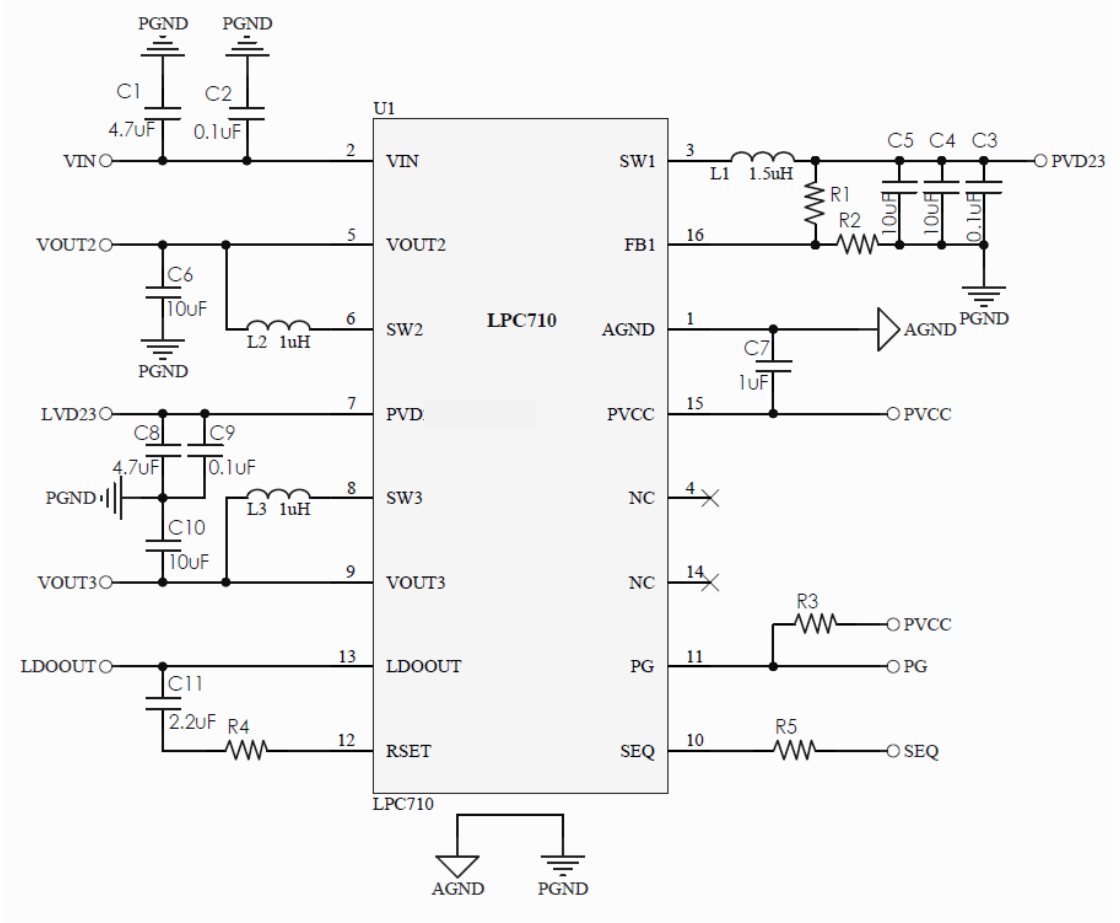
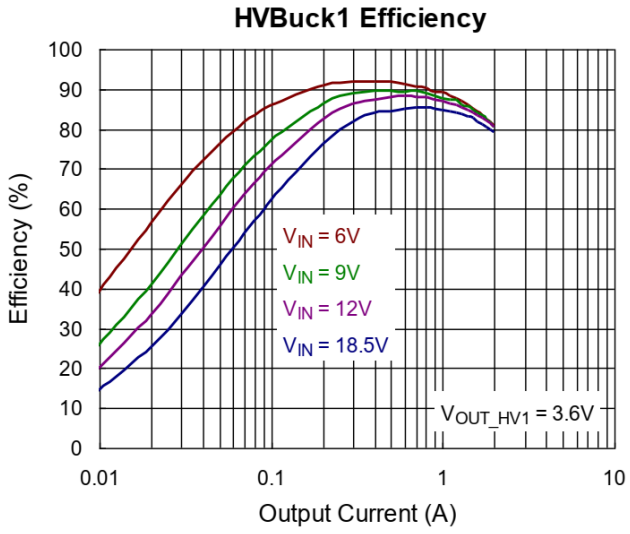
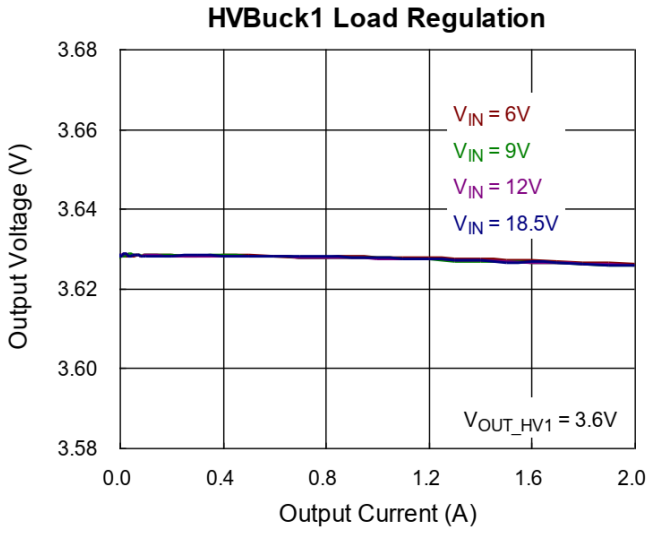
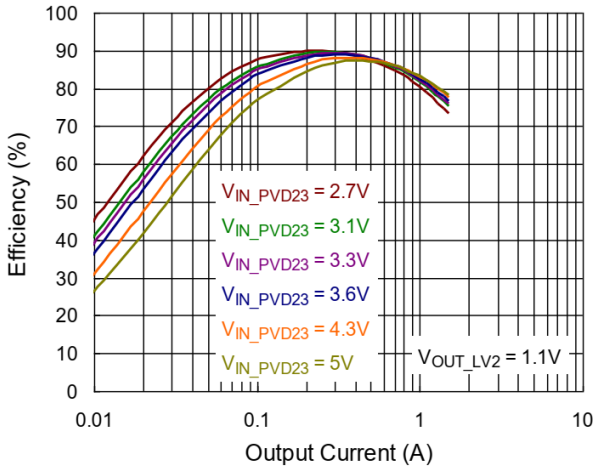



Figure 1. Typical Application

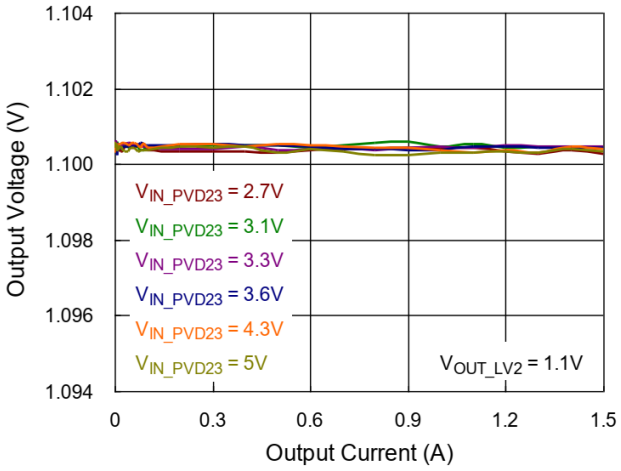


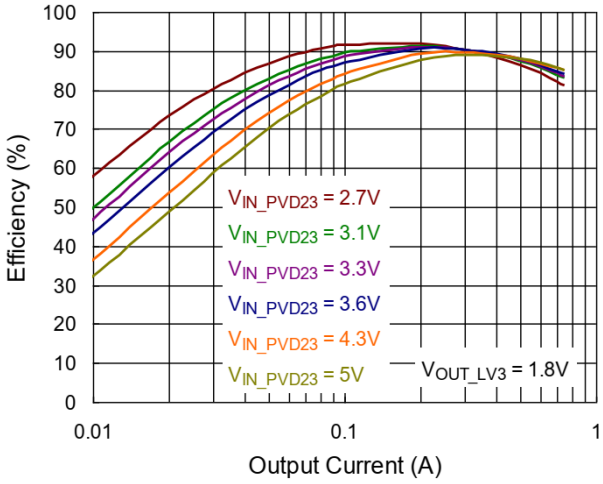
**LVBuck2 Efficiency**



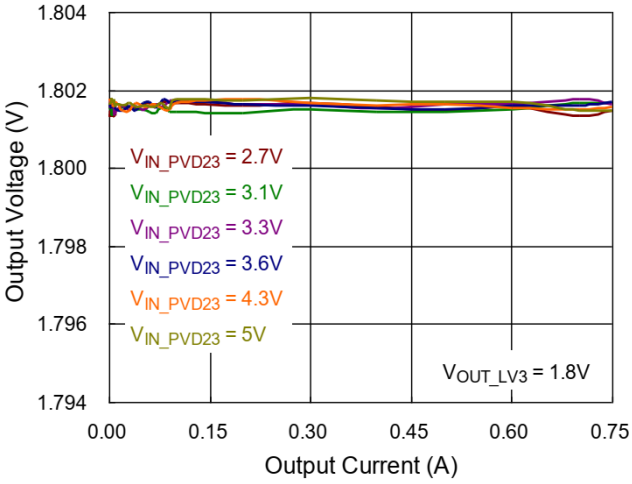

**LVBuck2 Load Regulation**



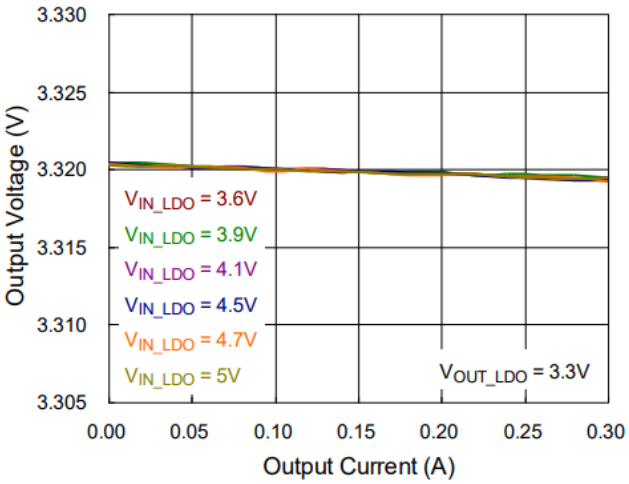

**LVBuck3 Efficiency**



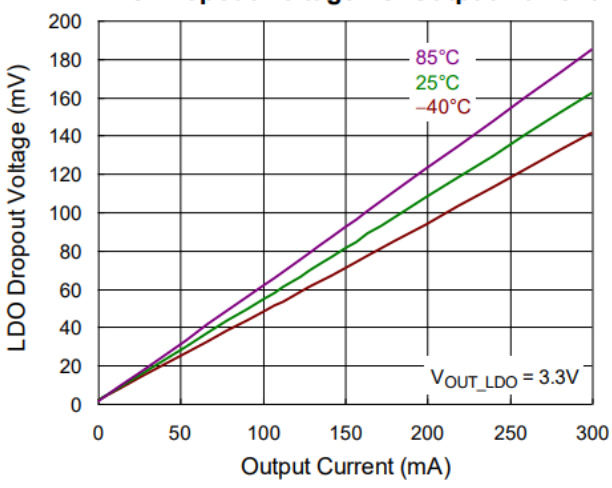

**LVBuck3 Load Regulation**



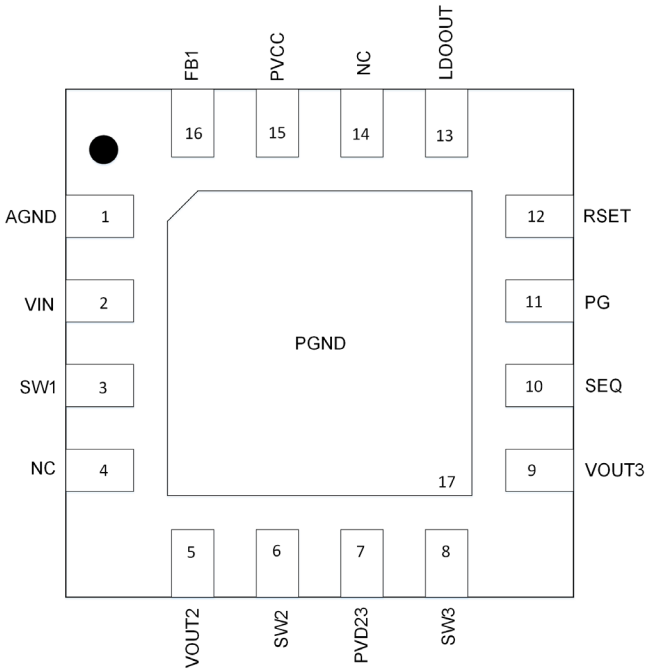

**LDO Load Regulation**




**LDO Dropout Voltage vs. Output Current**



## Pin Configuration




QFN-16 (3mm x 3mm)

## Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | AGND | Analog ground. |
| 2 | VIN | Supply voltage input of HVBuck1. Connect a 4.7uF or larger decouple ceramic capacitor between this pin and ground |
| 3 | SW1 | HVBuck1 switch node. |
| 4 | NC | Connect to ground |
| 5 | VOUT2 | Output voltage feedback input of LVBuck2. Directly connect the output capacitor node to this pin for better regulation. |
| 6 | SW2 | LVBuck2 switch node. |
| 7 | PVD | Supply voltage input of LVBuck2 and LVBuck3. Connect a 4.7uF or larger decouple ceramic capacitor between this pin and ground. |
| 8 | SW3 | LVBuck3 switch node |
| 9 | VOUT3 | Output voltage feedback input of LVBuck3. Directly connect the output capacitor node to this pin for better regulation. |
| 10 | SEQ | Power sequence selection |
| 11 | PG | Power status indication pin with open drain structure for HVBuck1, LVBuck2, LVBuck3 and LDO. PG at high state indicates all outputs work well. |
| 12 | RSET | LDO output voltage selection |
| 13 | LDOOUT | LDO output. Connect a 2.2uF ceramic decouple capacitor between this pin and ground. |
| 14 | NC | Connect to ground |

| | | |
|---|---|---|
| 15 | PVCC | Internal analog power output. Connect a 1μF ceramic decouple capacitor between this pin and ground. Note additional external loading on this pin is forbidden. |
| 16 | FB1 | Output voltage feedback input of HVBuck1. |

## ABSOLUTE MAXIMUM RATINGS

- VIN---------- -0.3V to 24V
- SW1---------- -0.3V to 24V
- VOUT2, PVD, VOUT3, SEQ, PG, RSET, LDOOUT, PVCC, FB1---------- -0.3V to 6.5V
- SW2, SW3---------- -0.3V to 6.5V
- Power Dissipation, PD @Ta=25℃ QFN-16L 3x3 ---------- 4.16W
- Package Thermal Resistance
  VQFN-16L 3x3, θJA ---------- 30℃/W
  VQFN-16L 3x3, θJC ---------- 4.4℃/W
- Lead Temperature (Soldering, 10 sec.)---------- 260°C
- Junction Temperature----------150°C
- Storage Temperature ---------- -65~150°C
- ESD Susceptibility HBM---------- 2KV

Recommended

- Supply Voltage , VIN---------- 4V to 18V
- Supply Voltage , VPVD, VLDOIN---------- 2.7V to 5V
- Ambient Temperature Range---------- -40~125°C
- Junction Temperature Range---------- -40~150°C

## Electrical Characteristics

($T_A$ = $T_J$ = –40°C to 125°C, $V_{IN}$ = 6V, $V_{OUT\_HV1}$ = 3.6V, $V_{OUT\_LV2}$ = 1.1V, $V_{OUT\_LV3}$ = 1.8V, $V_{OUT\_LDO}$ = 3.3V, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| System | | | | | | |
| Under-Voltage Lockout Threshold | UVLO_H | VIN rising | 3.6 | 3.8 | 4 | V |
| | UVLO_L | VIN falling | 3.15 | 3.3 | 3.45 | V |
| Input Over-Voltage Protection | VIN_OV | | 18.6 | 20 | 21.5 | V |
| Oscillator | | | | | | |
| Switching Frequency | Fsw | FREQUENCY[1] = 0 | 2 | 2.2 | 2.4 | MHz |
| | | FREQUENCY[1] = 1 | 3 | 3.3 | 3.6 | |
| Minimum On Time | $t_{ON\_MIN}$ | | | 48 | | ns |
| Minimum Off Time | $t_{OFF\_MIN}$ | | | 40 | | ns |
| CH1 HVBUCK1 | | | | | | |
| Input Voltage Range | VIN | | 4 | -- | 18.5 | V |
| Output Voltage Range | $V_{OUT\_HV1}$ | Buck mode operation. Switching frequency, minimum on time and minimum off time need to be considered. | 2.7 | -- | 5 | V |
| Output Feedback Voltage Accuracy | VFB1 | | 0.788 | 0.8 | 0.812 | V |
| High-Side MOSFET On Resistance | $R_{ON\_HS\_HV1}$ | From VIN pin to SW1 pin | 115 | 210 | 340 | mΩ |
| Low-Side MOSFET On Resistance | $R_{ON\_LS\_HV1}$ | From SW1 pin to PGND pin | 40 | 110 | 200 | mΩ |
| Inductor Peak Current Limit | $I_{CL\_PK\_HV1}$ | | 2.4 | 3 | 3.6 | A |
| Inductor Valley Current Limit | $I_{CL\_VL\_HV1}$ | | -- | 2.7 | -- | A |
| Negative Inductor Peak Current Limit | $I_{CL\_NPK\_HV1}$ | | 1 | 2.5 | 4 | A |
| Output Discharge Resistor | $R_{DIS\_HV1}$ | | 230 | 270 | 360 | Ω |
| Output Under-Voltage Falling Threshold | UVP_F_HV1 | | 40 | 50 | 60 | % |
| Output Feedback Over-Voltage Rising Threshold | OVP_R_HV1 | | -- | 110 | -- | % |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CH2 LVBUCK2 (VIN_PVD = 3.6V) | | | | | | |
| Input Voltage Range | VIN_PVD | | 2.7 | -- | 5 | V |
| Output Voltage | VOUT_LV2 | | -- | 1.1 | -- | V |
| Output Voltage Accuracy | VOUT_ACC_LV2 | | -1 | -- | 1 | % |
| High-Side MOSFET On Resistance | RON_HS_LV2 | From PVD pin to SW2 pin | 110 | 150 | 215 | mΩ |
| Low-Side MOSFET On Resistance | RON_LS_LV2 | From SW2 pin to PGND pin | 60 | 90 | 145 | mΩ |
| Inductor Peak Current Limit | ICL_PK_LV2 | | 1.8 | 2.2 | 2.6 | A |
| Inductor Valley Current Limit | ICL_VL_LV2 | | -- | 1.8 | -- | A |
| Negative Inductor Peak Current Limit | ICL_NPK_LV2 | | 0.7 | 1.7 | 2.9 | A |
| Output Discharge Resistor | RDIS_LV2 | | 6 | 9 | 4 | Ω |
| Output Under-Voltage Falling Threshold | UVP_F_LV2 | | 40 | 50 | 60 | % |
| Output Feedback Over-Voltage Rising Threshold | OVP_R_LV2 | | -- | 120 | -- | % |
| Output Over-Voltage Falling Threshold | OVP_F_LV2 | | -- | 110 | -- | % |
| Input Over-Voltage Rising Threshold | OVP_IN_R_LV2 | | 5.35 | 5.8 | 6.25 | V |
| Input Over-Voltage Hysteresis | OVP_IN_HYS_LV2 | VIN_PVD falling | -- | 580 | -- | mV |
| CH3 LVBuck3 (VIN_PVD = 3.6V) | | | | | | |
| Input Voltage Range | VIN_PVD | | 2.7 | -- | 5 | V |
| Output Voltage | VOUT_LV3 | | -- | 1.8 | -- | V |
| Output Voltage Accuracy | VOUT_ACC_LV3 | | -1 | -- | 1 | % |
| High-Side MOSFET On Resistance | RON_HS_LV3 | | 240 | 310 | 440 | mΩ |
| Low-Side MOSFET On Resistance | RON_LS_LV3 | | 170 | 230 | 360 | mΩ |
| Inductor Peak Current Limit | ICL_PK_LV3 | | 0.96 | 1.2 | 1.44 | A |
| Inductor Valley Current Limit | ICL_VL_LV3 | | -- | 1.08 | -- | A |
| Negative Inductor Peak Current Limit | ICL_NPK_LV3 | | 0.7 | 1.7 | 2.9 | A |
| Output Discharge Resistor | RDIS_LV3 | | 7 | 10 | 15 | Ω |
| Output Under-Voltage Falling Threshold | UVP_F_LV3 | | 40 | 50 | 60 | % |
| Output Feedback Over-Voltage Rising Threshold | OVP_R_LV3 | | -- | 120 | -- | % |
| Output Over-Voltage Falling Threshold | OVP_F_LV3 | | -- | 110 | -- | % |
| Input Over-Voltage Rising Threshold | OVP_IN_R_LV3 | | 5.35 | 5.8 | 6.25 | V |
| Input Over-Voltage Hysteresis | OVP_IN_HYS_LV3 | | -- | 580 | -- | mV |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CH4 LDO (VIN_PVD = 3.6V) | | | | | | |
| Input Voltage Range | VIN_PVD | | 2.7 | -- | 5 | V |
| Output Voltage Range | VOUT_LDO | VOUT_LDO setting via RSET | 1.8 | -- | 3.5 | V |
| Output Voltage Accuracy | VOUT_ACC_LDO | V IOUT_LDO IN_LDO - = 0mA to 300mA VOUT_LDO > 0.3V, | -1 | -- | 1 | % |
| Maximum Output Current | IOUT_MAX_LDO | | 300 | -- | -- | mA |
| Dropout Voltage | VDROP_LDO | IOUT_LDO = 300mA (Note 5) | -- | -- | 300 | mV |
| Output Current Limit | ICL_LDO | | 345 | 450 | 555 | mA |
| Output Discharge Resistor | RDIS_LDO | | 48 | 76 | 104 | Ω |
| Output Under-Voltage Falling Threshold | UVP_F_LDO | | 40 | 50 | 60 | % |
| Output Feedback Over-Voltage Rising Threshold | OVP_R_LDO | | -- | 125 | -- | % |
| Output Over-Voltage Falling Threshold | OVP_F_LDO | | -- | 110 | -- | % |
| Input Over-Voltage Rising Threshold | OVP_IN_R_LDO | | 5.35 | 5.8 | 6.25 | V |
| Input Over-Voltage Hysteresis | OVP_IN_HYS_LDO | | -- | 500 | -- | mV |
| PVCC | | | | | | |
| Internal Regulator Output Voltage | VOUT_PVCC | | 4.33 | 4.58 | 4.83 | V |
| Over-Current Limit | ICL_PVCC | | 150 | -- | 300 | mA |
| Power Good | | | | | | |
| Pull Down Voltage | VOUT_L_PG | Current into PG pin equal to 5mA | -- | -- | 200 | mV |
| Input Leakage Current | ILEAK_PG | 1.8V applied on PG pin | -- | -- | 1 | μA |
| Timing | | | | | | |
| Soft-Start Time | tSS_HV1 | Time from VOUT_HV1 0% rise to 90% of target value, no load | 500 | 1000 | 1500 | us |
| | tSS_LV2 | Time from VOUT_LV2 0% rise to 90% of target value, no load | 500 | 1000 | 1500 | |
| | tSS_LV3 | Time from VOUT_LV3 0% rise to 90% of target value, no load | 500 | 1000 | 1500 | |
| | tSS_LDO | Time from the previous turn on channel's output voltage reaching 90% of target value to VOUT_LDO rise to 90% of target value. | 200 | 700 | 1100 | |
| PG Delay Time | tDLY_PG | | 9 | 10 | 11 | ms |

## System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. ($T_A$ = $T_J$ = –40°C to 125°C, $V_{IN}$ = 6V, $V_{OUT\_HV1}$ = 3.6V, $V_{OUT\_LV2}$ = 1.1V, $V_{OUT\_LV3}$ = 1.8V, $V_{OUT\_LDO}$ = 3.3V, unless otherwise specified.)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| System | | | | | | |
| Over-Temperature Protection | OTP | | -- | 160 | -- | °C |
| Over-Temperature Protection Hysteresis | OTP_H | | -- | 20 | -- | °C |
| CH1 HV BUCK1 | | | | | | |
| Maximum Output Current | IOUT_MAX_HV1 | | 2 | -- | -- | A |
| Load Regulation | VLOAD_REG_HV1 | IOUT_HV1 = 0A to 2A | -- | -- | 0.1 | %/A |
| Line Regulation | VLINE_REG_HV1 | VIN = 5V to 18.5V, IOUT_HV1 = 2A | -- | -- | 1 | % |
| Load Transient | VLOAD_TRAIN_HV1 | IOUT_HV1 = 10mA to 500mA to 10mA, 1μs | –150 | -- | 150 | mV |
| Line Transient | VLINE_TRAIN_HV1 | VIN = 5V to 18.5V to 5V, 100μs,IOUT_HV1 = 10mA/500mA | –50 | -- | 50 | mV |
| Output Ripple | VRIPPLE_HV1 | Peak to peak in one switching cycle | -- | -- | 20 | mVpp |
| CH2 LV BUCK2 | | | | | | |
| Maximum Output Current | IOUT_MAX_LV2 | | 1.5 | -- | -- | A |
| Load Regulation | VLOAD_REG_LV2 | IOUT_LV2 = 0A to 1.5A | -- | -- | 0.1 | %/A |
| Line Regulation | VLINE_REG_LV2 | VIN_PVD = 2.7V to 5V, IOUT_LV2 = 1.5A | -- | -- | 1 | % |
| Load Transient | VLOAD_TRAIN_LV2 | IOUT_LV2 = 10mA to 500mA to 10mA, 1μs | –50 | -- | 50 | mV |
| Line Transient | VLINE_TRAIN_LV2 | VIN_PVD = 3V to 5V to 3V, 50μs, IOUT_LV2 = 10mA/1A | –50 | -- | 50 | mV |
| Output Ripple | VRIPPLE_LV2 | Peak to peak in one switching cycle | -- | -- | 10 | mVpp |
| CH3 LV BUCK3 | | | | | | |
| Maximum Output Current | IOUT_MAX_LV3 | | 0.75 | -- | -- | A |
| Load Regulation | VLOAD_REG_LV3 | IOUT_LV3 = 0A to 750mA | -- | -- | 0.1 | %/A |
| Line Regulation | VLINE_REG_LV3 | VIN_PVD = 2.7V to 5V, IOUT_LV3 = 750mA | -- | -- | 1 | % |
| Load Transient | VLOAD_TRAIN_LV3 | IOUT_LV3 = 10mA to 300mA to 10mA, 1μs | –50 | -- | 50 | mV |
| Line Transient | VLINE_TRAIN_LV3 | VIN_PVD = 3V to 5V to 3V, 50μs, IOUT_LV3 =10mA/300mA | –50 | -- | 50 | mV |
| Output Ripple | VRIPPLE_LV3 | Peak to peak in one switching cycle | -- | -- | 10 | mVpp |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LDO | | | | | | |
| Power Supply Rejection Ratio | PSRR_LDO | IOUT_LDO = 100mA, f = 100kHz | -- | 60 | -- | dB |
| | | IOUT_LDO = 100mA, f = 2MHz | -- | 55 | -- | |
| Output Noise Voltage | EN_LDO | Iout_LDO=100mA, f=100Hz to 100KHz | -- | 60 | -- | μV |
| Load Transient | VLOAD_TRAIN_LDO | IOUT_LDO = 10mA to 200mA to 10mA, 1μs | -25 | -- | 25 | mV |
| Line Transient | VLINE_TRAIN_LDO | All VOUT_LDO, VIN_LDO step 600mV, LDO not in dropout condition, 10μs, IOUT_LDO = 1mA/300mA | -25 | -- | 25 | mV |
| Component Requirement | | | | | | |
| Input Capacitance | CIN_HV1 | | 1.5 | 4.7 | 10 | uF |
| | CIN_PVD | | 1.5 | 4.7 | 10 | |
| Output Capacitance | COUT_HV1 | | 3.3 | 10 | 14 | uF |
| | COUT_LV2 | | 4.5 | 10 | 14 | |
| | COUT_LV3 | | 4.5 | 10 | 14 | |
| | COUT_LDO | | 0.7 | 2.2 | 4 | |
| Output Inductance | LHV1 | | 1 | 1.5 | 2 | uH |
| | LLV2 | | 0.68 | 1 | 1.2 | |
| | LLV3 | | 0.68 | 1 | 1.2 | |
| PVCC Capacitance | CPVCC | | 0.3 | 1 | 1.4 | μF |

**Note 1.** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
**Note 2.** $\theta_{JA}$ is measured under natural convection (still air) at $T_A$ = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $\theta_{JC}$ is measured at the exposed pad of the package.
**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.
**Note 4.** The device is not guaranteed to function outside its operating conditions.
**Note 5.** Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
**Note 6.** PVCC is the pre-regulator output voltage only for internal circuitry. External loading on PVCC pin is forbidden

## Function Block Diagram

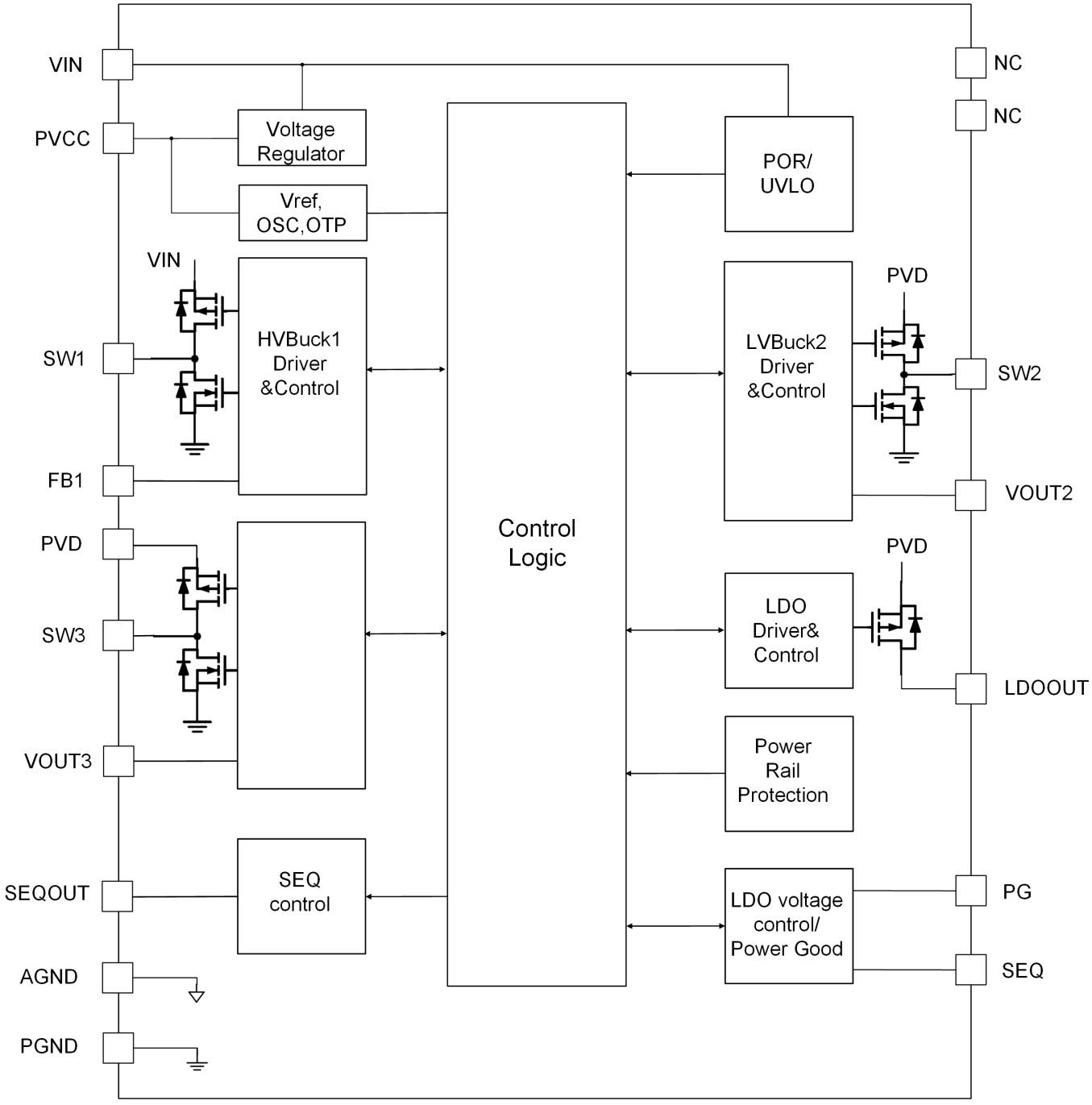



Figure3: Block Diagram

## Operation

The LPC710 is a highly integrated power-management integrated circuit (PMIC) for automotive camera system,

which includes three step-down converters (CH1 HVBuck1, CH2 LVBuck2, CH3 LVBuck3) and one generic LDO (CH4 LDO).

**System Under-Voltage Protection and Over-Voltage Protection**

The LPC710 stops operating if VIN voltage falls below the Under-Voltage Lock Out level (UVLO_L). There is a typical 500mV hysteresis implemented to avoid unstable on/off behaviors. The shift values of UVLO_H and UVLO_L both toward to the same direction. (To positive or negative at the same time.) The device is initialized in its default state after VIN voltage recovering from UVLO_H. When VIN voltage reaches the Over-Voltage Protection level, the DC/DC converters, LDO are disabled immediately. Then the IC enters into latch off state and only can re-start with VIN ON/OFF. Meanwhile, the PG status will be also set to 0V to indicate IC fault condition

Bucks1, 2, 3, and LDO. Buck2 and Buck3 output voltages are sensed at the VOUT2 and VOUT3 pins respectively, while LDO is sensed at the LDOOUT pin. Buck1 UV and OV sensing uses the PVD input pin; Buck1 output regulation uses the FB1 input pin. This separation on Buck1 provides protection against cases where the feedback path is interrupted because of events such as an opened solder joint.

**Thermal Protection**

The LPC710 features an over- temperature protection (OTP). When the junction temperature is higher than 160°C typical value, OTP is triggered to disable all outputs and the device enters into a latch off state. When the LPC710 recovers from OTP, the device only can re-start with VIN ON/OFF.

**Pre-Regulator**

The device integrates a 4.45V linear regulator (PVCC) supplied by VIN to provide power to the internal circuitry. The PVCC can be used as the RSET and SEQ pull-up supply but it is “NOT” allowed to power other device or circuitry. A 1uF decoupling capacitor must be connected between PVCC and AGND to filter the noise and it needs to be placed as close as possible to the PVCC pin.

**Peak Current Mode Control**

The three step-down converters utilize the peak current mode control. An internal oscillator initiates turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. With comparisons of the inductor peak current signal during high-side MOSFET switch on interval and the internal compensation signal derived from the sensed feedback voltage with reference voltage, the high-side MOSFET switch is turned off and inductor current continues to flow through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, the regulated inductor current controls duty-cycle and output voltage of the converter.

**Spread-Spectrum Operation**

Due to the periodicity of the switching signal, the energy concentrates in one particular frequency and its harmonics. The energy is radiated and possible to result in a potential EMI issue. The LPC710 equips a spread-spectrum function to meet CISPR and automotive EMI compliances. The spread-spectrum function is implemented by a pseudo random sequence, the spread range and modulation rate set by register of the switching frequency. For example, when the switching frequency typical value is 2.2MHz, the frequency range varies from 2.0MHz to 2.4MHz. Therefore, the LPC710 can guarantee that the 2.2MHz switching frequency does not drop into the 1.8MHz AM band limit.

**Phase-Shifted Operation**

The LPC710 supports phase shift operations among the step-down converters for further easing the simultaneous switching energy radiation quantity. The internal clock is automatically shifted to different respective sub-clocks for step-down converters. For example, when two step-down converters application, the beginning turn-on time between two high-side MOSFETs will have a 180- degree phase difference. Likewise, a 120-degree phase difference when three step-down converters.

**Allowable Channel Floating**

For saving PCB layout space and material cost, the unused low-voltage step-down converter (CH2/CH3) is allowable to pin (SW2/SW3) floating without any inductor and output capacitor placement. The pin PVD is required to connect to a fixed voltage for floating detection and it is allowable without capacitor placement. The LPC710 automatically detects pin status during power-on procedure to determine whether the channel is used or not. In addition, the related failures on unused channels do not affect the device operation.

**Power Good Indication**

The LPC710 features an open-drain power- good output (PG) to monitor the output voltage status. Connect a pull-up resistor from PG pin to an external voltage. Note it is forbidden to use PVCC as pulled-up voltage of PG pin. When the last channel of power-on sequence reaches 90% of its target output voltage, the PG signal is pulled up to indicate “Power Good” status after 10ms tills to device disabled or any other protection happens.

**External Control Output**

The LPC710 features an open-drain external control output (SEQ) for external device. Connect a pull-up resistor from SEQ pin to an external voltage. Note it is forbidden to use PVCC as pulled-up voltage of SEQ pin. Referring to Table 1 for further information about power-on sequence.

## Application Information

**Power Sequence Control**

The LPC710 supports 6 power-on sequences for the step-down converters and LDO via the dedicated resistor on SEQ pin. SEQ pin is not allowable at floating state and resistance selected out of range is not guaranteed to correct power-on sequence. In addition, there is only simultaneous power-off for all outputs. To fix the resistor selection on SEQ pin before enabling the device. Any change during the power on procedure is not guarantee to the correct power-on sequence. Below table shows the power-on sequence with its corresponding resistance.

**Table 1 Power- on sequence control**

| SEQ NO. | Resistance on SEQ | | | Sequence | | | |
|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | | | | |
| SEQ0 | 1.07M | 1.1M | 1.13M | CH1 | CH2 | CH3 | CH4 |
| SEQ1 | 319k | 330k | 341k | CH1 | CH2 | CH4 | CH3 |
| SEQ2 | 164k | 169k | 174k | CH1 | CH3 | CH2 | CH4 |
| SEQ3 | 81.6k | 84.5k | 87.4k | CH1 | CH3 | CH4 | CH2 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SEQ4 | 45.4k | 47k | 48.6k | CH1 | CH4 | CH2 | CH3 |
| SEQ5 | 26.1k | 27k | 27.9k | CH1 | CH4 | CH3 | CH2 |

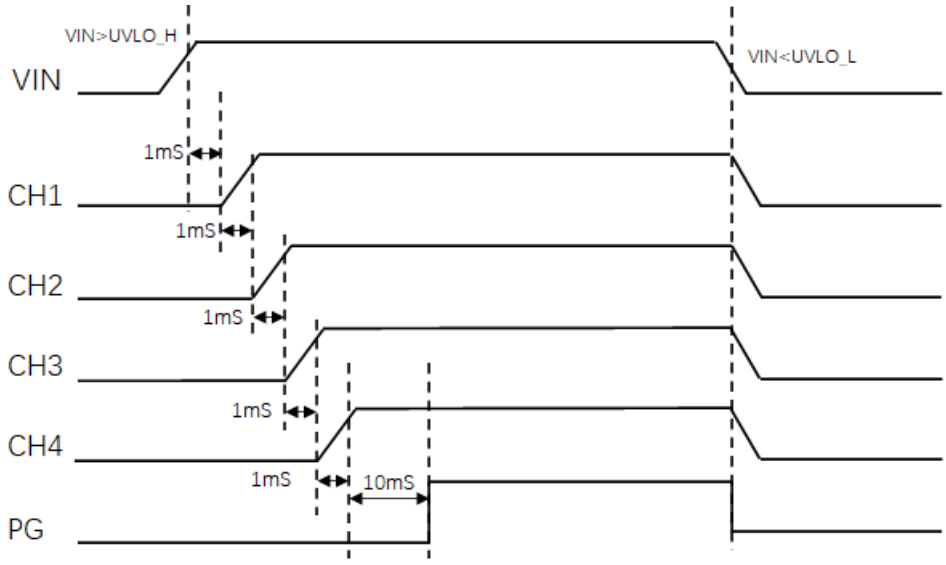



Figure 3. Example SEQ0

**Output Voltage Setting**

**HVBuck1**
The output voltage set by external feedback resistors expressed in the following equation.

$V_{OUT\_HV1} = (1 + R1/R2) \times V_{FB1}$

Where the reference voltage $V_{FB1}$ is 0.8V (typ.) The placement of the resistive divider should be as close as possible to the FB1 pin. For better output voltage accuracy, the divider resistors with ±1% tolerance or better should be used. The resistance ranges from few kΩ to hundreds of kΩ is recommended.

**LVBuck2 and LVBuck3**
The output voltage of LVBuck2 is fixed 1.1V as default.
The output voltage of LVBuck3 is fixed 1.8V as default.

**LDO**
The LDO output voltage is controlled by setting the dedicated resistor on RSET pin. RSET pin is not allowable at floating state and resistance selected out of range is not guaranteed to correct output voltage. Changing of the output voltage real time is not recommended. To fix the resistor selection on RSET pin before enabling the device.

**Table 2 LDO Output Voltage**

| RSET No | Resistor on REST (Ω) | | | V |
|---|---|---|---|---|
| | Min | Typ | Max | |
| RSET0 | 1.07M | 1.1M | 1.13M | 3.5 |
| RSET1 | 319k | 330k | 341k | 3.4 |
| RSET2 | 164k | 169k | 174k | 3.2 |

| | | | | |
|---|---|---|---|---|
| RSET3 | 81.6k | 84.5k | 87.4k | 3.1 |
| RSET4 | 45.4k | 47k | 48.6k | 3.0 |
| RSET5 | 26.1k | 27k | 27.9k | 2.8 |
| RSET6 | 14.5k | 15k | 15.5k | 2.7 |
| RSET7 | 7.78k | 8.06k | 8.34k | 1.8 |
| RSET8 | Short to PVCC | | | 2.9 |
| RSET9 | Short to PGND | | | 3.3 |

**Channel Protection Features**
The LP700 equips protections to prevent the device from damages causing by abnormal operations or fault conditions. (Over-load, Short-circuit, Soldering issue…etc.)

- **Under-Voltage Protection for output voltage (UVP)**

■ **HVBuck1, LVBuck2, LVBuck3 and LDO**
The device disables all channels and enters into latch off state if step-down converter or LDO output under voltage fault detected continuously over deglitch time and the device only can re-start with VIN>3.8V.

- **Over-Voltage Protection (OVP)**

■ **HVBuck1**
When FB1 pin over-voltage fault detected, the high-side and low-side MOSFETs turn off immediately, PG flag will assert, auto-recover to switch until FB1 pin's voltage decrease to the reset level, PG flag will de-assert.

■ **LVBuck2, LVBuck3 and LDO**
The device disables all channels when step-down converter or LDO output over-voltage fault detected continuously over deglitch time. When the fault released, the device auto-restarts all channels in sequence.

- **Over-Current Protection (OCP)**

■ **HVBuck1, LVBuck2 and LVBuck3**
The step-down converter includes a cycle-by-cycle high-side MOSFET peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. If an over-current condition occurs, the controller will immediately turn off the high-side MOSFET and turn on the low-side MOSFET to prevent the inductor current exceeding the peak current limit level. After inductor current decreasing to below the valley current limit, the high-side MOSFET resume switching on. If over-current fault further detected continuously over than deglitch time, the device disables all channels and enters into latch off state and the device only can re-start with VIN ON/ OFF. When the fault released, the device auto-restarts all channels in sequence.

■ **LDO**
When the load reaches the current limit threshold, the current sent to the output will keep at current limit level. If over-current fault detected continuously over than the deglitch time, the device disables all channels and enters into latch off state and the device only can re-start with VIN ON/ OFF.
When the fault released, the device auto-restarts all channels in sequence.

- **Input Over-Voltage Protection (OVP)**

■ **LVBuck2, LVBuck3 and LDO**

If the input voltage of step-down converters (LVBuck2, LVBuck3) or LDO reaches over-voltage protection level, the device disables all channels. After fault removed, it auto-restarts all channels in sequence.

**Table3. Protection List**

| Channel | Type | Threshold (Typ.) | Deglitch Time (Typ.) | Channels Behavior | Reset and Threshold (Typ.) |
|---|---|---|---|---|---|
| Base | BIST | NA | NA | All channel stay disable | |
| System | UVLO | $V_{IN}$ ≤ 3.3V (after IC Operation) | 32μs | Disable all channels | $V_{IN}$ ≥ 3.8V |
| | OVP | $V_{IN}$ ≥ 20V | 5ms | Disable all channels then latch-off protection | $V_{IN}$ ≤ 3.3V, then $V_{IN}$ ≥ 3.8V |
| | OTP | $T_J$ ≥ 160°C | 5μs | Disable all channels then latch-off protection | $T_J$ ≤ 140°C and $V_{IN}$ ≤ 3.3V, then $V_{IN}$ ≥ 3.8V |
| CH1 HVBuck1 | UVP | PVD ≤ 0.8V x 50% | 5μs | Disable all channels then latch-off protection | $V_{IN}$ ≤ 3.3V, then $V_{IN}$ ≥ 3.8V |
| | OVP | PVD ≥ 0.8V x 110% | NA | High MOSFETs off, low-side MOSFET conditionally ON . | **$V_{FB\_OVP}$** < 0.8V x 110% |
| | OCP | $I_{L1\_peak}$ ≥ 3A | 10ms | Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection. | If latch-off protection, $V_{IN}$ ≤ 3.3V, then $V_{IN}$ ≥ 3.8V |
| CH2 LVBuck2 | UVP | $V_{OUT\_LV2}$ ≤ 1.1V x 50% | 5μs | Disable all channels then latch-off protection | $V_{IN}$ ≤3.3V then $V_{IN}$ ≥3.8V |
| | OVP | $V_{OUT\_LV2}$ ≥ 1.1V x 120% | 5ms | Disable all channels | $V_{OUT2}$ ≤ 1.1V x 110% with deglitch 5ms |
| | OCP | $I_{L2\_peak}$ ≥ 2A | 10ms | Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection. | If latch-off protection, $V_{IN}$ ≤ 3.3V, then $V_{IN}$ ≥ 3.8V |
| | Input OVP | $V_{IN\_PVD}$ ≥ 5.8V | 5μs | Disable all channels | $V_{IN\_PVD}$ ≤ 5.22V with deglitch 5us |
| CH3 LVBuck3 | UVP | $V_{OUT\_LV3}$ ≤ 1.8V x 50% | 5μs | Disable all channels then latch-off protection | $V_{IN}$ ≤3.3V then $V_{IN}$ ≥3.8V |
| | OVP | $V_{OUT\_LV3}$ ≥ 1.8V x 120% | 5ms | Disable all channels | $V_{OUT3}$ ≤ 1.8V x 110% with Deglitch 5ms |
| | OCP | $I_{L3\_peak}$ ≥ 2A | 10ms | Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection. | If latch-off protection, $V_{IN}$ ≤ 3.3V, then $V_{IN}$ ≥ 3.8V |
| | Input OVP | $V_{IN\_PVD}$ ≥ 5.8V | 5μs | Disable all channels | $V_{IN\_PVD}$ ≤ 5.22V with deglitch 5us |
| CH4 LDO | UVP | $V_{OUT\_LDO}$≤$V_{OUT\_LDO}$ setting x 40% | 5μs | Disable all channels then latch-off protection | $V_{IN}$ ≤3.3V then $V_{IN}$ ≥3.8V |
| | OVP | $V_{OUT\_LDO}$ ≥ $V_{OUT\_LDO}$ x 125% | 5ms | Disable all channels | $V_{OUT\_LDO}$ ≤ $V_{OUT\_LDO}$ x 110% with deglitch 5ms |
| | OCP | $I_{OUT\_LDO}$ ≥ 450mA | 10ms | Disable all channels then latch-off protection | $V_{IN}$ ≤ 3.3V, then $V_{IN}$ ≥ 3.8V |
| | Input OVP | $V_{IN\_LDO}$ ≥ 5.8V | 5μs | Disable all channels | V with deglitch 5 $V_{IN\_LDO}$ ≤ 5.3Vμs |

**Input and Output Capacitor Selection**

- **HVBuck1, LVBuck2 and LVBuck3**

It is recommended at least a 4.7μF input capacitor with a 10μF output capacitor for step-down converters. The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output ripple can be calculated as below.

$$\Delta V_{OUTRipple} = \Delta V_{ESR} + \Delta V_{OUT} = \Delta V_{ESR} + \frac{\Delta I_L}{8 \times Cout \times fsw}$$

where $\Delta V_{ESR} = I_{Crms} \times R_{cesr}$

- **LDO**

Like any low dropout regulator, the external capacitor of the LPC710 must be carefully selected for regulator stability and performance. Using a 2.2μF capacitor for the LDO's input and output is suitable. Additional capacitor paralleled on the output may get better noise suppression but also lead to higher input inrush current when LDO outputs. It should be taken into consideration carefully.

**Thermal Considerations**

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following
formula :

$$P_{D(max)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature;
$T_A$ is the ambient temperature; and $\theta_{JA}$ is the junction-to-ambient thermal resistance. For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a QFN-16L 3x3 package, the thermal resistance, $\theta_{JA}$, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four layer test

board. The maximum power dissipation at $T_A$ = 25°C can be calculated as below:

$$P_{D(MAX)} = \frac{(150℃ - 25℃)}{(30℃/W)} = 4.16W$$

for a QFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

## Power Control

### No Supply:
The PMIC's input pin has UVLO_L detection circuit, if the input voltage VIN is lower than the UVLO_L rising threshold, the PMIC's all functions are disabled.

### Power On
The bucks and LDO are on. The PG pin switches high while the outputs are within the defined thresholds

### Power Off:
All power rails are power off. When VIN is lower than its rising UVLO_L, the system will enter power off state first.

### High Efficiency Buck Regulator
Buck1 to Buck3 are synchronous step-down DC/DCs which have built-in UVLO, soft-start, compensation and hiccup current limit protection. The switching clock is CCM operation.

### Power Supply and UVLO
Vin is the power supply of Buck1 the bias and internal logic blocks. FB1 is the feedback of Buck1, and the power supply for Buck 2, Buck3 and LDOOUT.

### Internal Soft-Start
The soft start function is implemented to prevent the PMIC output voltage from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage. At this point, the reference voltage takes over.

### Diagnostics
The LPC710 integrates several diagnostic features in order to improve system safety. If enabled, several built in self-test functions will run in the power off state before power on begins. Analog built in self-test (ABIST) ensures proper operation of the over voltage and under voltage comparators. If any diagnostic functions detect a failure, the power good flag will assert. Once the fault has been cleared, the power good flag will de-assert.

The first reference (REF1) is the reference for output regulation, provided internal compensation. The second reference (REF2) is used by the OV and UV comparators, when the error of the internal compensation network or REF1 is greater than REF2, the comparators will turn off the switch, the power good flag will assert. If the reference comes back into compliance and the fault register is cleared, the power good flag will de-assert.

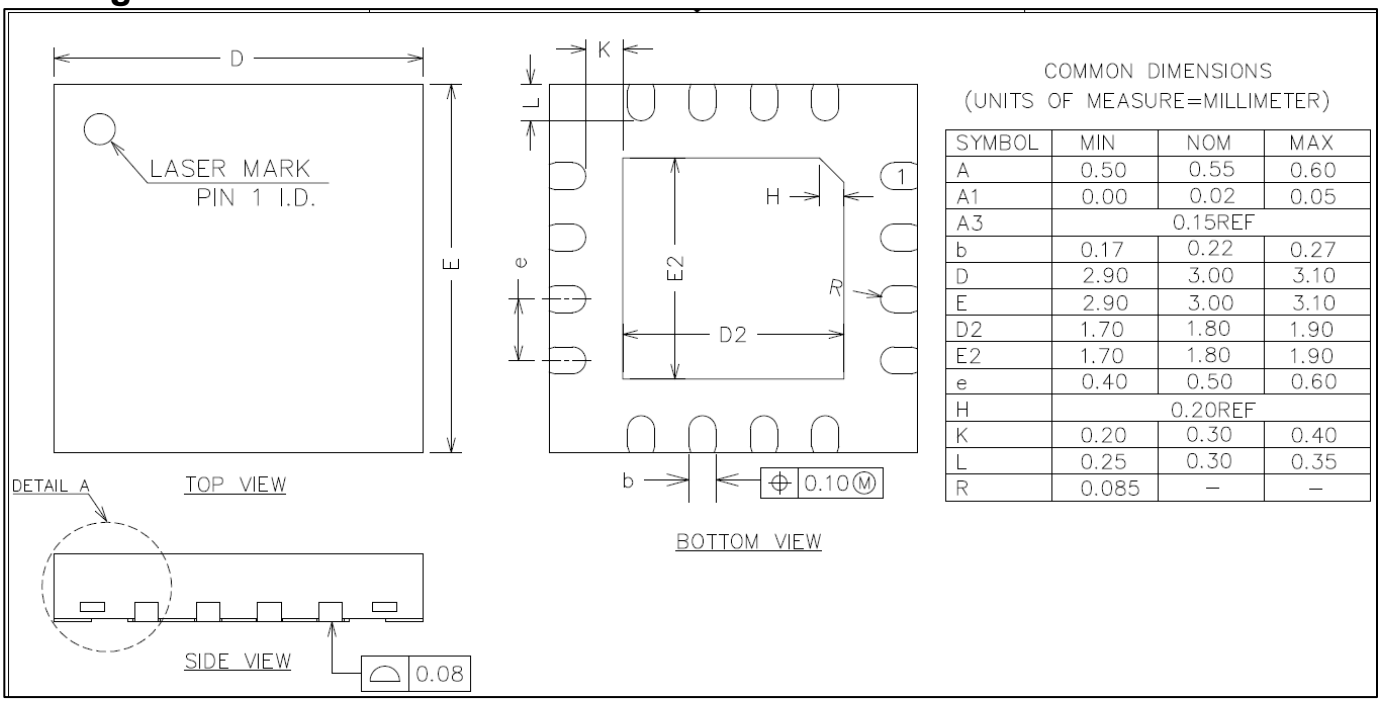
### Power Good
The power good pin is a open drain output. It will indicate logic high if the device is powered on, all outputs are within the power good range, and all fault registers are cleared.  The Power Good is an active low output that provides a reset (low) signal to the system MCU when a fault occurs.

### Layout Considerations

The PCB layout is an important step to maintain the high performance of the LPC710. Both the high current and the fast switching nodes demand full attention to the PCB layout to keep the robustness of the LPC710 through the PCB layout. Improper layout might lead to the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the LPC710, the following PCB layout guidelines must be strictly followed.

- The trace from switching node to inductor should be as short as possible to minimized the switching loop for better EMI.
- Place the input and output capacitors close to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- Connect the AGND and PGND to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the step-down converter's output capacitor to the feedback network to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

## Package Information




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.15REF | |
| b | 0.17 | 0.22 | 0.27 |
| D | 2.90 | 3.00 | 3.10 |
| E | 2.90 | 3.00 | 3.10 |
| D2 | 1.70 | 1.80 | 1.90 |
| E2 | 1.70 | 1.80 | 1.90 |
| e | 0.40 | 0.50 | 0.60 |
| H | | 0.20REF | |
| K | 0.20 | 0.30 | 0.40 |
| L | 0.25 | 0.30 | 0.35 |
| R | 0.085 | – | – |

### Revision History

| Revision Number | Date of Release | Changes |
|---|---|---|
| 1.0 | | 1: Preliminary |