LMP6911PJZF 30V P-Channel MOSFET

Features

- -60V/-3.1A, $R_{DS(ON)}$<190mΩ@V_{GS}=-10V
- Improved dv/dt capability
- Fast switching
- 100% EAS Guaranteed
- Green Device Available
- SOT-23 package design

Product Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

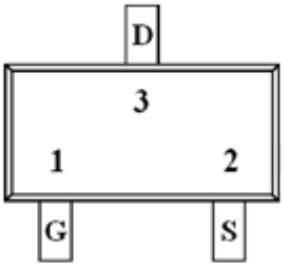
These devices are well suited for high efficiency fast switching applications.

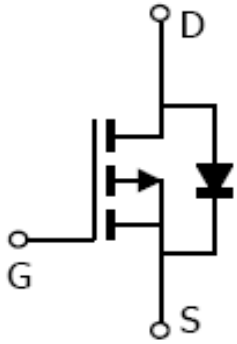
Applications

- Motor Drive
- Power Tools
- Led Lighting

Pin Configuration

LMP6911PJZF (SOT-23)





PIN	Description
1	Gate
2	Source
3	Drain

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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP6911PJZF	LMP6911P	JZ	F	SOT-23	3000

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
M XWMM	M	XWMM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-60	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A=25℃	-3.1	A
		T_A=100℃	-2	
I_{DM}	Pulsed Drain Current		-12.4	A
EAS	Single Pulse Avalanche Energy		32	mJ
IAS	Single Pulse Avalanche Current		-8	A
P_D	Power Dissipation (T_A=25℃)		1.56	W
	Power Dissipation (Derate above 25℃)		0.012	W/℃
T_J	Operating Junction Temperature Range		-50 to +150	℃
T_{STG}	Storage Temperature Range		-50 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		80	℃/W

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-60			V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃, I_D=-1mA		-0.05		V/℃
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.2	-1.9	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient			5		mV/℃
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-60V, V_{GS}=0V			-1	uA
		V_{DS}=-48V, V_{GS}=0V, T_J=125℃			-10	
I_S	Continuous Source Current	V_G=V_D=0V, Force Current			-3.1	A
I_{SM}	Pulsed Source Current				-12.4	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-3A		160	190	mΩ
		V_{GS}=-4.5V, I_D=-1.5A		200	240	
g_{FS}	Forward Transconductance	V_{DS}=-10V, I_D=-3A		3.5		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=-1A			-1	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=-30V,V_{GS}=-10V, I_D=-3A		8.2	12	nC
Q_{gs}	Gate-Source Charge			1.8	3.6	
Q_{gd}	Gate-Drain Charge			1.5	3	
C_{iss}	Input Capacitance	V_{DS}=-30V,V_{GS}=0V, f=1MHz		425	615	pF
C_{oss}	Output Capacitance			35	50	
C_{rss}	Reverse Transfer Capacitance			20	30	
$t_{d(on)}$	Turn-On Time	V_{DD}=-30V,I_D=-1A, V_{GS}=-10V,R_G=6Ω		5.2	10	ns
t_r				19	36	
$t_{d(off)}$	Turn-Off Time			35	67	
t_f				10.6	20	

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Typical Performance Characteristics

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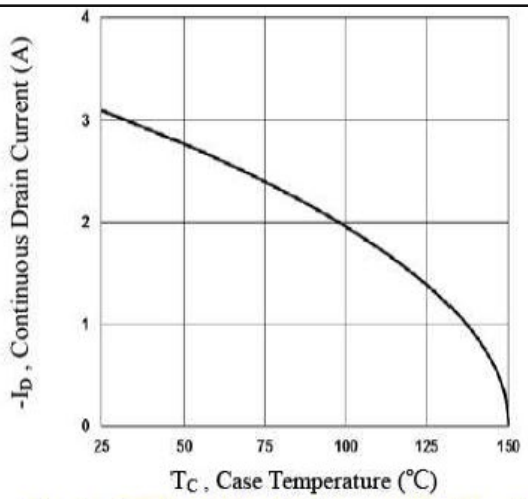

Fig.1 Continuous Drain Current vs. T_c

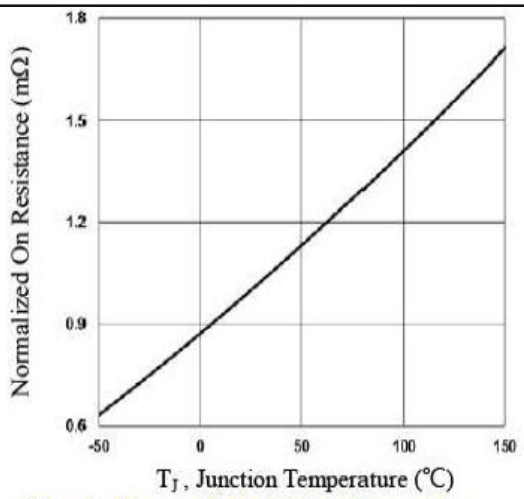

Fig.2 Normalized RDSON vs. T_J

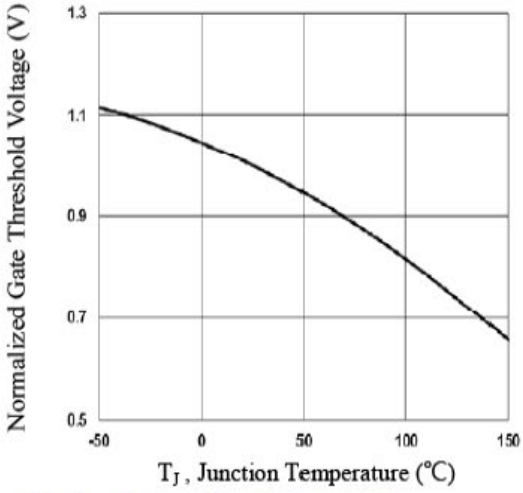

Fig.3 Normalized V_{th} vs. T_J

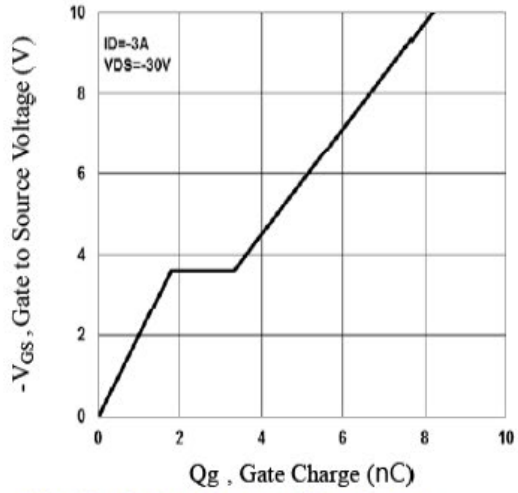

Fig.4 Gate Charge Waveform

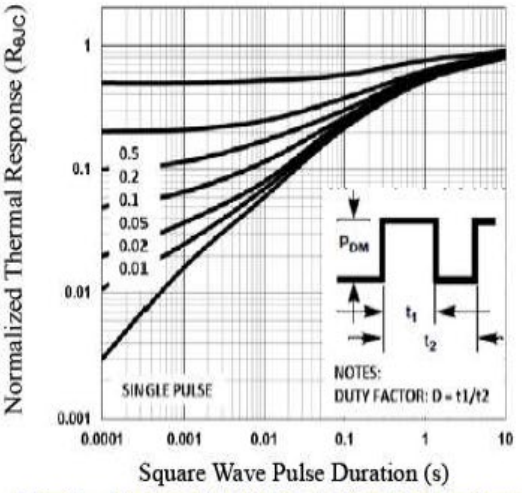

Fig.5 Normalized Transient Impedance

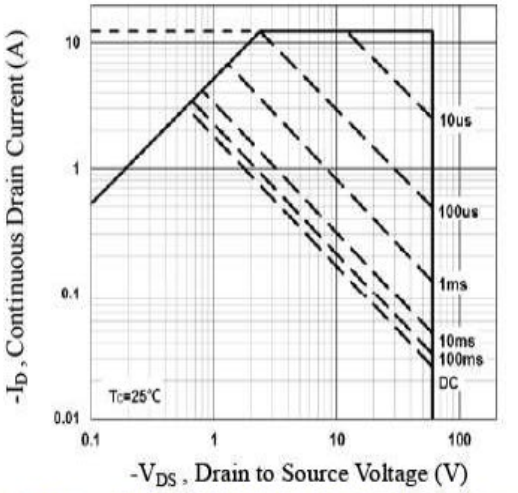

Fig.6 Maximum Safe Operation Area

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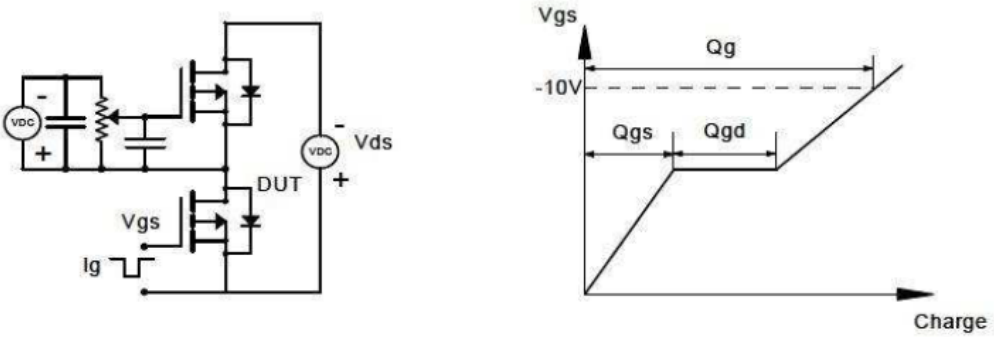
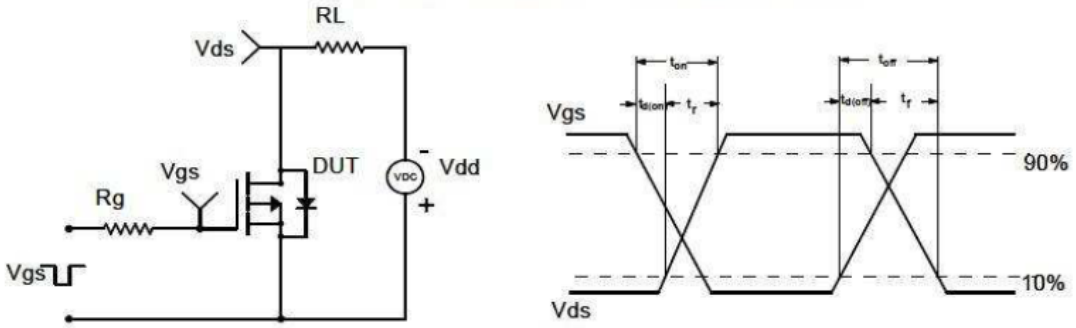
Typical Performance Characteristics(continue)

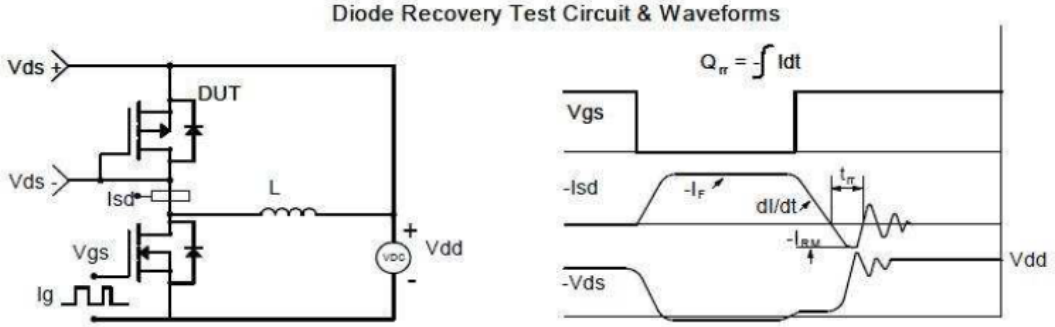
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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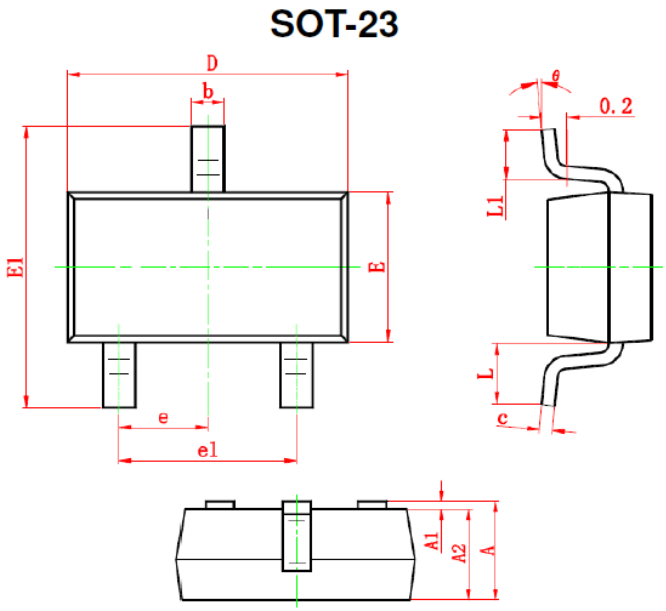
Package Dimension:



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0º	8º	0º	6º

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