

**LMP3825ETF 30V P-Channel MOSFET**
**Features**

- -30V/-0.5A,  $R_{DS(ON)} < 2500m\Omega @ V_{GS} = -4.5V$
- -30V/-0.2A,  $R_{DS(ON)} < 2900m\Omega @ V_{GS} = -2.5V$
- -30V/-0.1A,  $R_{DS(ON)} < 5000m\Omega @ V_{GS} = -1.8V$
- Low-Voltage Operation
- High-Speed Circuits
- ESD Protection
- DFN1006-3L package design

**Product Description**

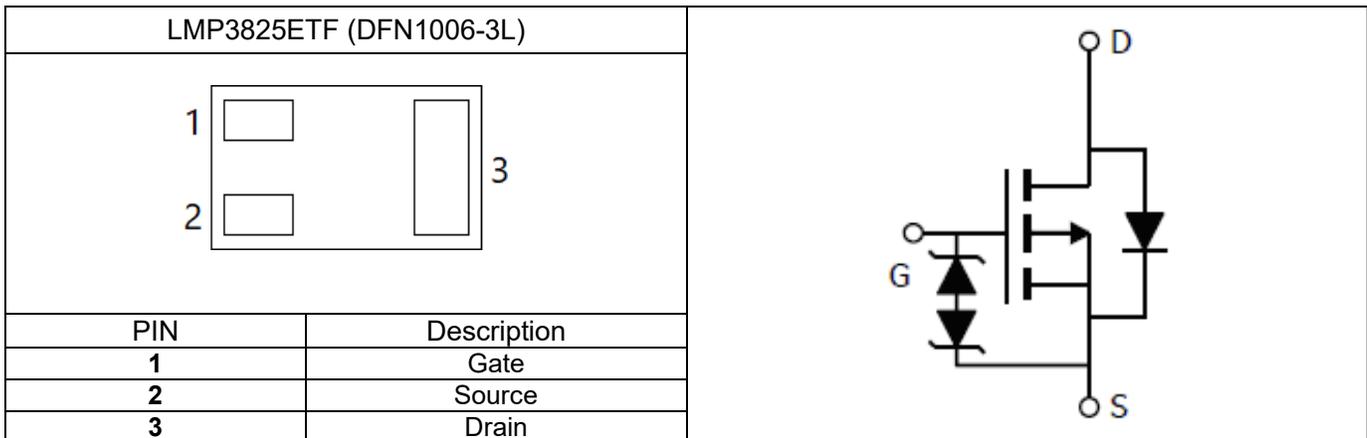
LMP3825ETF, P-Channel enhancement mode MOSFET,

uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low gate charge.

These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

**Applications**

- Drivers, Relays, Solenoids, Lamps, Hammers
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Smart Phones, Pagers

**Pin Configuration**


**Ordering Information**

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3825ETF	LMP3825E	T	F	DFN1006-3L	10000

**Marking Information**

Marking Information		
Part Marking	Part Number	LFC code
5XWM	5	XWM

**Absolute Maximum Ratings**

 (T<sub>C</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V <sub>DSS</sub>	Drain-Source Voltage	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	±10	V
I <sub>D</sub>	Continuous Drain Current <sup>1</sup>	T <sub>A</sub> =25°C	-0.32
		T <sub>A</sub> =70°C	-0.26
I <sub>DM</sub>	Pulsed Drain Current	-1.2	A
P <sub>D</sub>	Power Dissipation <sup>1</sup>	0.4	W
R <sub>θJA</sub>	Thermal Resistance Junction to ambient <sup>1</sup>	315	°C/W
R <sub>θJA</sub>	Thermal Resistance Junction to ambient <sup>2</sup>	160	°C/W
T <sub>J</sub>	Operating Junction Temperature Range	-55 to +150	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C

Note1. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. Note2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

**Electrical Characteristics**

 (T<sub>C</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit.
<b>Static</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-0.4		-1.0	
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V			±10	uA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	uA
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-0.5A		1.5	2.5	Ω
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-0.2A		1.9	2.9	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-0.1A		2.4	5.0	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.5A		960		mS
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-0.5A, V <sub>GS</sub> =0V			1.3	V
<b>Dynamic</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A		1.0		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-8V, I <sub>D</sub> =-1A		0.2		
Q <sub>gd</sub>	Gate-Drain Charge			0.1		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz		54		pF
C <sub>oss</sub>	Output Capacitance			10.9		
C <sub>rss</sub>	Reverse Transfer Capacitance			5.8		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =-10V, R <sub>L</sub> =47Ω, I <sub>D</sub> =-0.2A, V <sub>GEN</sub> =-4.5V, R <sub>G</sub> =10Ω		3.8		ns
t <sub>r</sub>				11		
t <sub>d(off)</sub>	Turn-Off Time			45		
t <sub>f</sub>				20		

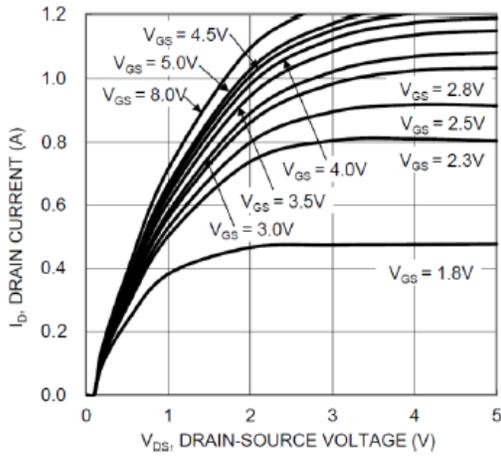
**Typical Performance Characteristics**


Fig. 1 Typical Output Characteristics

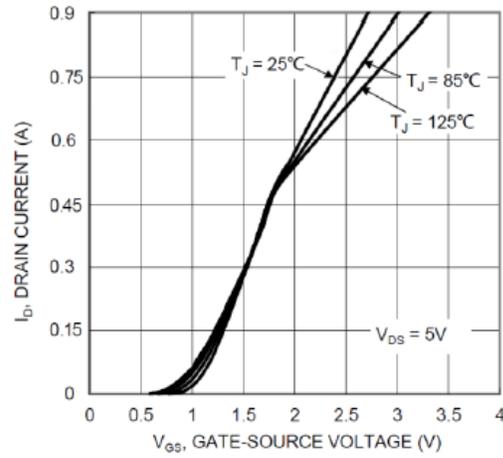
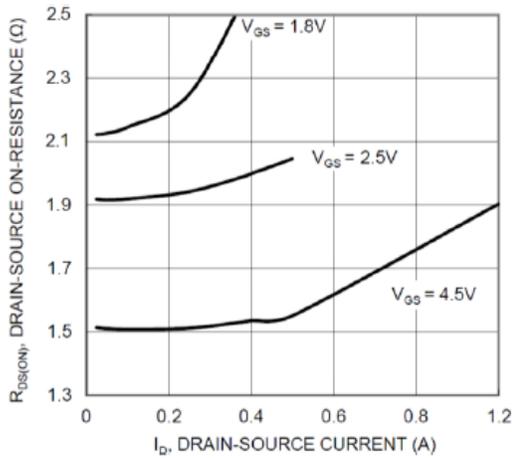
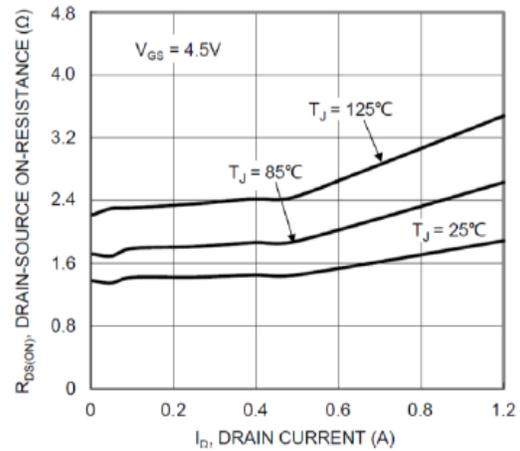
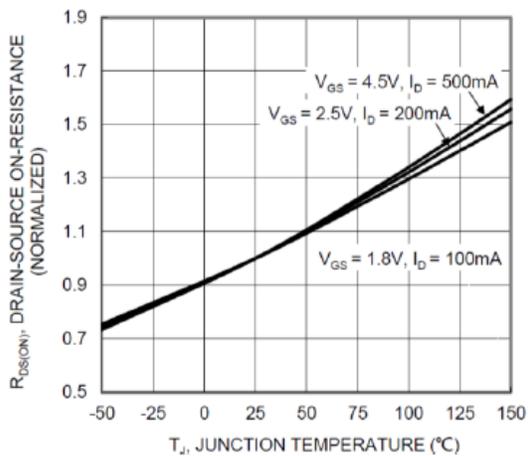
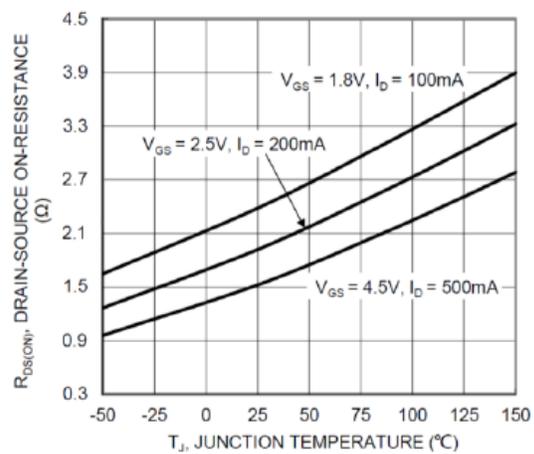


Fig. 2 Typical Transfer Characteristics


 Fig. 3 Typical On-Resistance vs.  $I_D$  and  $V_{GS}$ 

 Fig. 4 Typical Drain-Source On-Resistance vs.  $I_D$  and  $T_J$ 

 Fig. 5 On-Resistance Variation with  $T_J$ 

 Fig. 6 On-Resistance Variation with  $T_J$

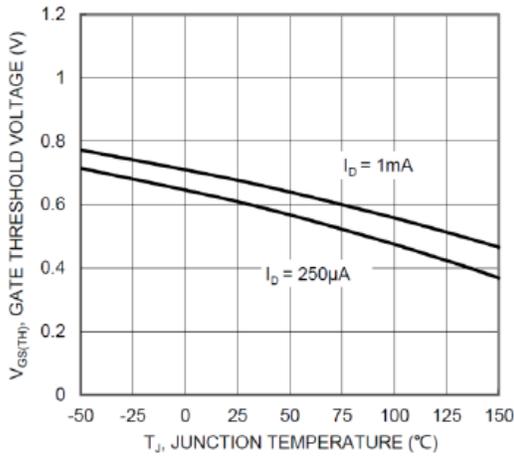
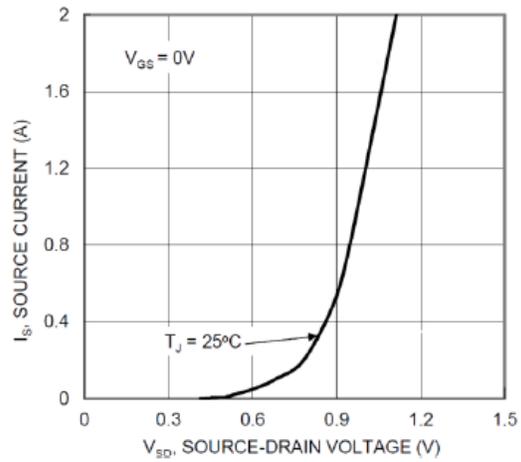
**Typical Performance Characteristics(continue)**

 Fig. 7 Gate Threshold Variation vs.  $T_A$ 


Fig. 8 Diode Forward Voltage vs. Current

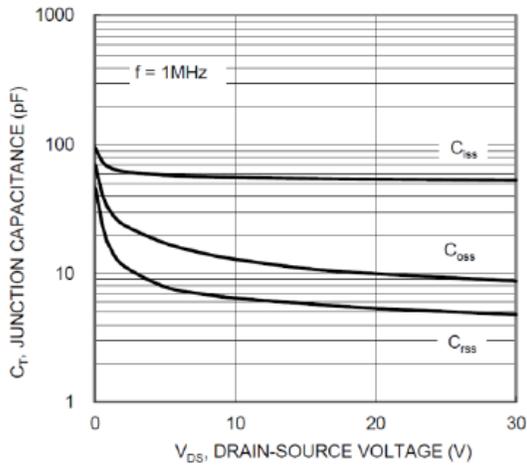


Fig. 9 Typical Capacitance

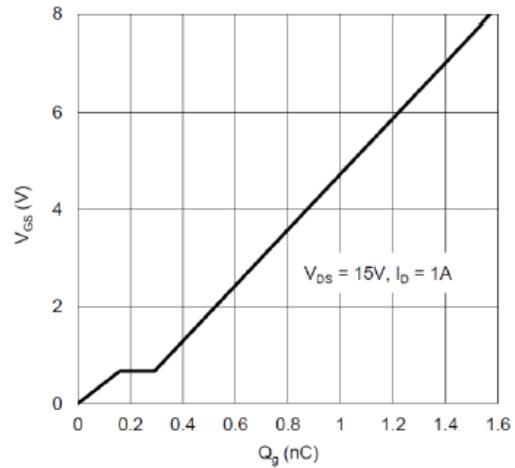


Fig. 10 Gate Charge

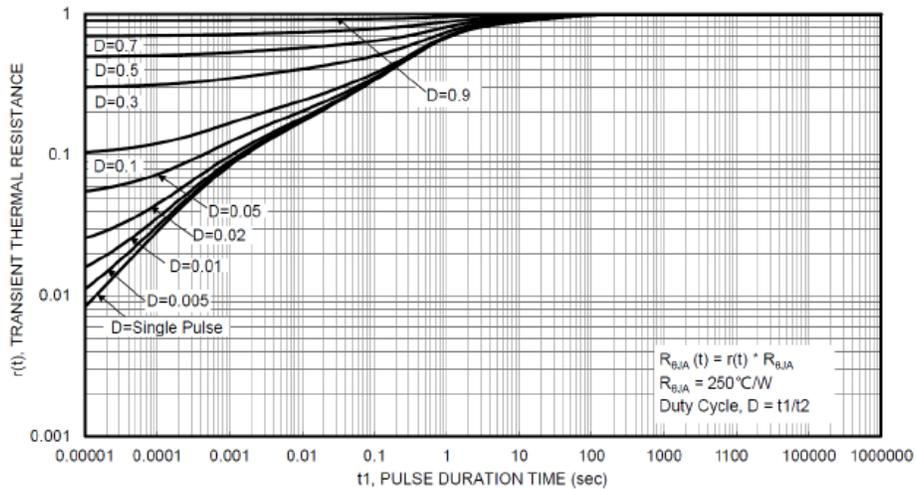
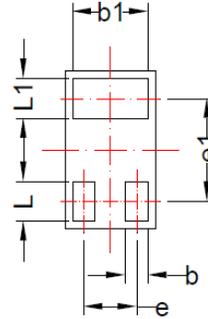
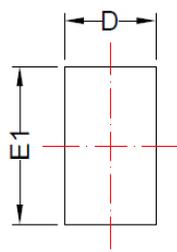
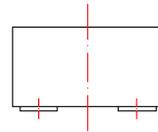
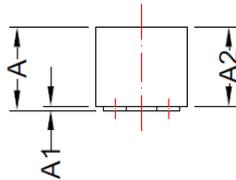


Fig. 11 Transient Thermal Response

**Package Dimension:**
**DFN1006-3L**

**BACKSIDE VIEW**


DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH, NOT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

<b>Dimensions</b>				
<b>SYMBOL</b>	<b>Millimeters</b>		<b>Inches</b>	
	<b>MIN</b>	<b>MAX</b>	<b>MIN</b>	<b>MAX</b>
<b>A</b>	0.45	0.60	0.018	0.024
<b>A1</b>	0.00	0.05	0.000	0.002
<b>A2</b>	0.40	0.60	0.016	0.024
<b>b</b>	0.10	0.20	0.004	0.008
<b>b1</b>	0.45	0.55	0.018	0.022
<b>D</b>	0.55	0.65	0.022	0.026
<b>E1</b>	0.95	1.05	0.037	0.041
<b>e</b>	0.35 BSC		0.014 BSC	
<b>e1</b>	0.65 BSC			
<b>L</b>	0.2	0.3	0.008	0.012
<b>L1</b>	0.2	0.3	0.008	0.012

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