LMP3153JZF 30V P-Channel MOSFET

Features

- -30V/-4.8A, $R_{DS(ON)}$<54mΩ@V_{GS}=-10V
- -30V/-3.8A, $R_{DS(ON)}$<72mΩ@V_{GS}=-4.5V
- -30V/-3.0A, $R_{DS(ON)}$<120mΩ@V_{GS}=-2.5V
- Suit for -4.5V Gate Drive Applications
- SOT-23 package design

Product Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

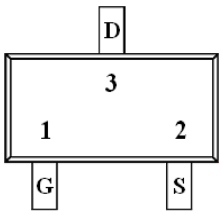
These devices are well suited for high efficiency fast switching applications.

Applications

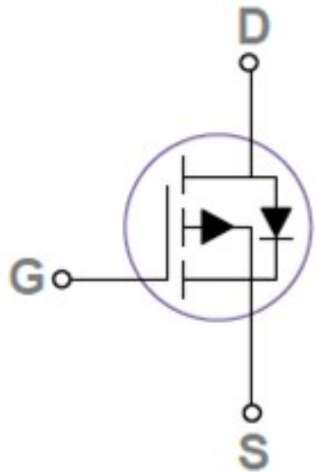
- Notebook
- LED display
- DC-DC System
- LDC Panel

Pin Configuration

LMP3153JZF (SOT-23)



PIN	Description
1	Gate
2	Source
3	Drain



Notice: The information in this document is subject to change without notice.

Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3153JZF	LMP3153	JZ	F	SOT-23	3000

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
31XWM	31	XWM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current (T_J=150℃)	T_A=25ºC	-4.8	A
		T_A=70ºC	-3.8	
I_{DM}	Pulsed Drain Current		-19	A
I_S	Continuous Source Current (Diode Conduction)		-1	A
P_D	Power Dissipation	T_A=25ºC	1.92	W
		T_A=70ºC	1.23	
T_J	Operating Junction Temperature		150	ºC
T_{STG}	Storage Temperature Range		-55/150	ºC
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient (t ≤ 10s)		65	ºC/ W

Notice: The information in this document is subject to change without notice.

Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.7		-1.3	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	uA
		V_{DS}=-24V, V_{GS}=0V, T_J=85ºC			-30	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-4.8A		44	54	mΩ
		V_{GS}=-4.5V, I_D=-3.8A		62	72	
		V_{GS}=-2.5V, I_D=-3.0A		98	120	
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.7	-1.0	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		573		pF
C_{oss}	Output Capacitance			74		
C_{rss}	Reverse Transfer Capacitance			53		
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_D=-4.8A		13.6		nC
Q_{gs}	Gate-Source Charge			1.2		
Q_{gd}	Gate-Drain Charge			2.0		
$t_{d(on)}$	Turn-On Time	V_{DD}=-15V, R_L=10Ω, I_D=-1.0A, V_{GEN}=-10V, R_G=6.0Ω		6.9		ns
T_r				12.3		
$t_{d(off)}$	Turn-Off Time			25		
T_f				13		

Notice: The information in this document is subject to change without notice.

Typical Performance Characteristics

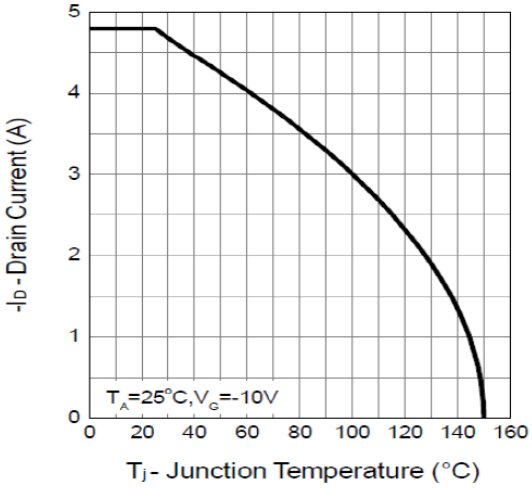


Figure 1. Drain Current vs. Temperature

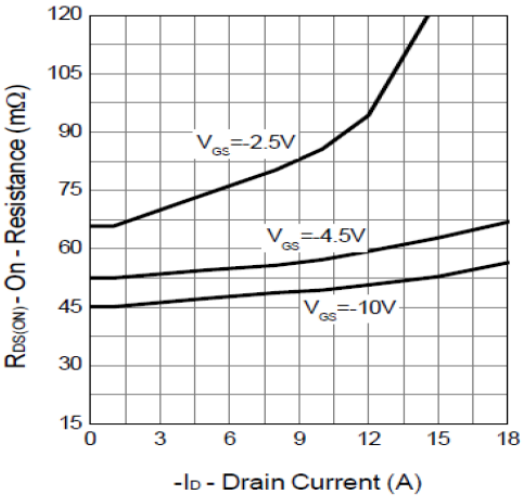


Figure 2. On-Resistance vs. Drain Current

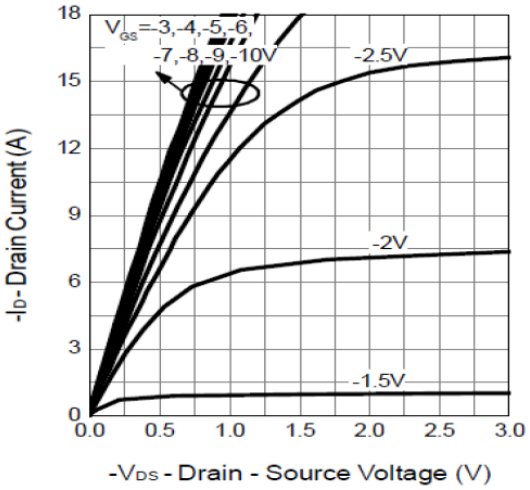


Figure 3. Output Characteristics

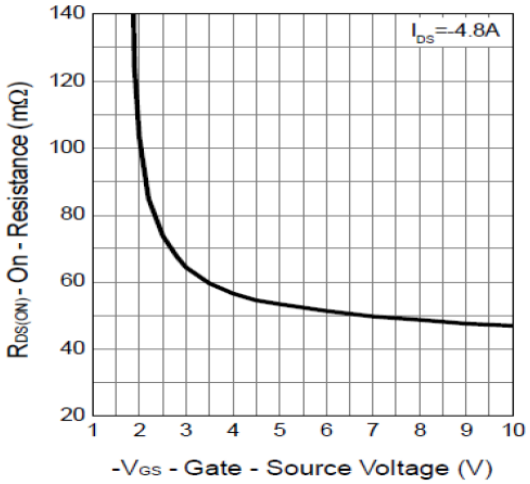


Figure 4. On-Resistance vs. Gate-Source Voltage

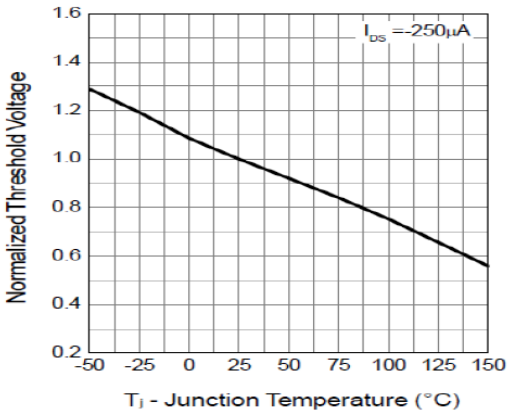


Figure 5. Threshold Voltage

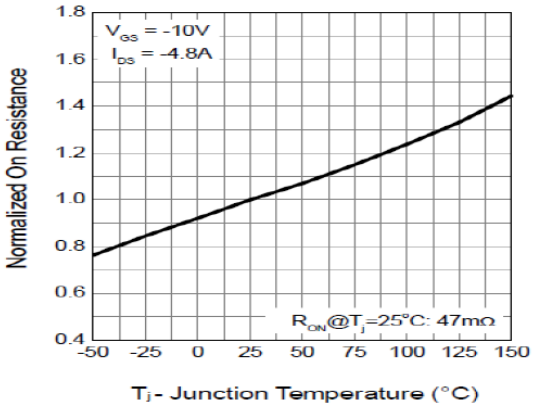


Figure 6. On-Resistance vs. Gate-Source Voltage

Notice: The information in this document is subject to change without notice.

Typical Performance Characteristics(continue)

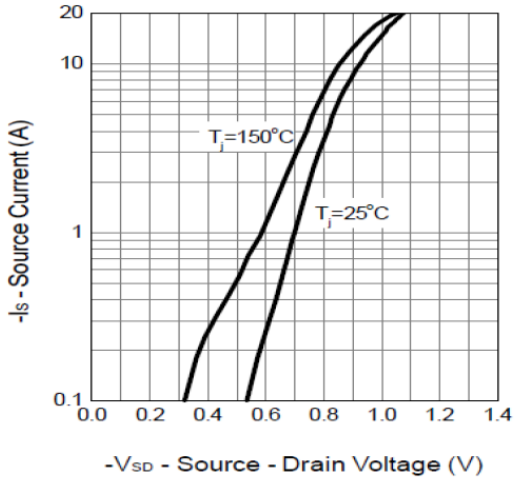


Figure 7. Source-Drain Diode Foward Voltage

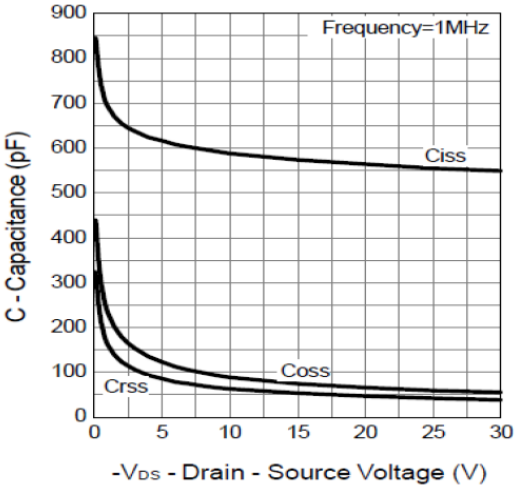


Figure 8. Capacitance

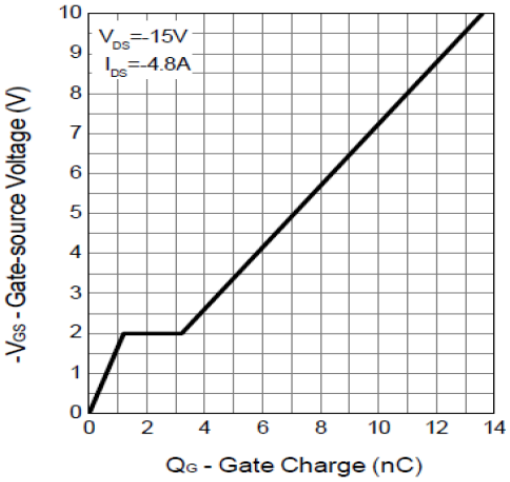


Figure 9. Gate Charge

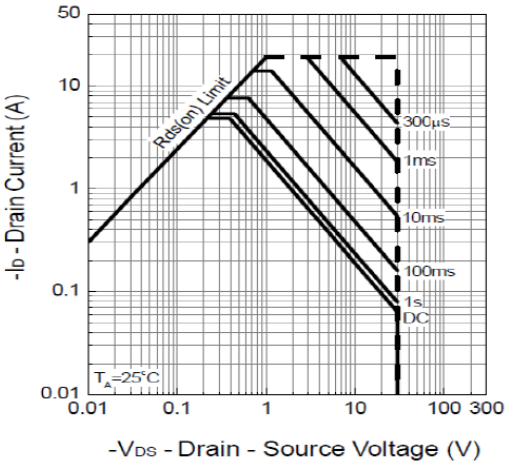


Figure 10. Safe Operation Area

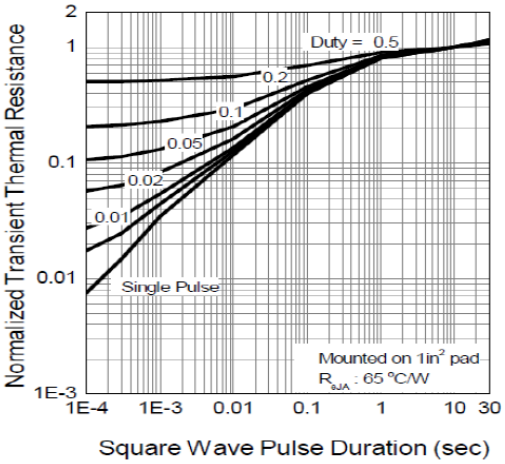
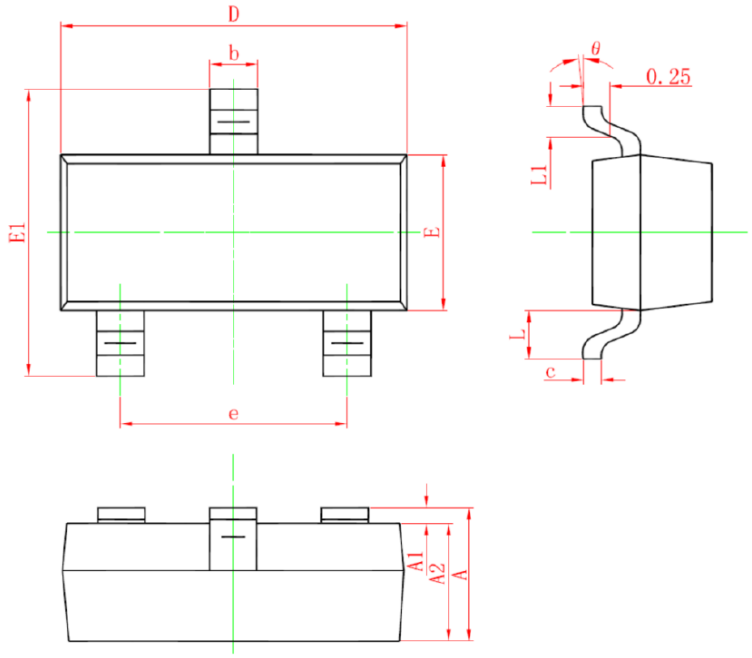


Figure 11. Normalized Thermal Transient Impedance

Notice: The information in this document is subject to change without notice.

Package Dimension:

SOT-23



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.043
b	0.300	0.500	0.012	0.020
c	0.132	0.202	0.005	0.008
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0º	8º	0º	8º

Notice: The information in this document is subject to change without notice.

NOTICE:

LFC Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all LFC Semiconductor products described or contained herein. LFC Semiconductor products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. LFC Semiconductor makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Information furnished is believed to be accurate and reliable. However LFC Semiconductor assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of LFC Semiconductor. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information without express written approval of LFC Semiconductor.

Notice: The information in this document is subject to change without notice.