LMP3131SF 30V P-Channel MOSFET

Features

- -30V/-5.7A, $R_{DS(ON)}$<32mΩ@V_{GS}=-10V
- Fast switching
- Suit for -4.5V Gate Drive Applications
- Green Device Available
- SOP-8 package design

Product Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

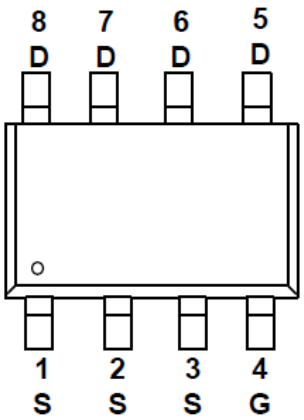
These devices are well suited for high efficiency fast switching applications.

Applications

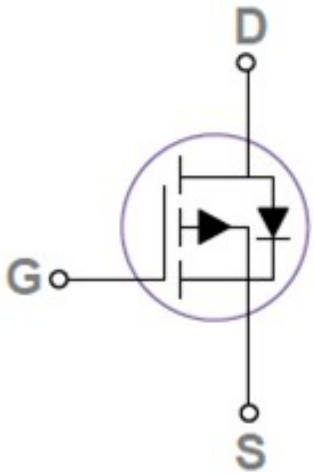
- Notebook
- Load Switch
- Battery Protection
- Hand-held Instruments

Pin Configuration

LMP3131SF (SOP-8)



PIN	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3131SF	LMP3131	S	F	SOP-8	4000

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
3131S XWMMMM	3131S	XWMMMM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A=25℃	-5.7	A
		T_A=70℃	-4.6	
I_{DM}	Pulsed Drain Current[1]		-22.8	A
EAS	Single Pulse Avalanche Energy[2]		39.2	mJ
IAS	Single Pulse Avalanche Current[2]		-28	A
P_D	Power Dissipation (T_A=25℃)		1.47	W
T_J	Operating Junction Temperature Range		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		85	℃/W

Note:
1. Repetitive Rating: Pulsed width limited by maximum junction temperature.

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	-1.3	-1.7	-2.3	V
I_{GSS}	Gate-Source Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-30V, V_{GS}=0V T_J=25℃			-1	uA
		V_{DS}=-24V, V_{GS}=0V, T_J=125℃			-10	
I_S	Continuous Source Current	V_G=V_D=0V,Force Current			-5.5	A
I_{SM}	Pulsed Source Current				-11	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=-4A		26	32	mΩ
		V_{GS}=4.5V, I_D=-3A,		42	46	
g_{FS}	Forward Transconductance	V_{DS}=-10V, I_D=-3A		5		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=-1A			-1	V
Dynamic						
Q_g	Total Gate Charge[2,3]	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-5A		8	15	nC
Q_{gs}	Gate-Source Charge[2,3]			3.3	6	
Q_{gd}	Gate-Drain Charge[2,3]			2.3	5	
C_{iss}	Input Capacitance	V_{DS}=15V,V_{GS}=0V, f=1MHz		757	1280	pF
C_{oss}	Output Capacitance			122	210	
C_{rss}	Reverse Transfer Capacitance			88	175	
$t_{d(on)}$	Turn-On Time[2,3]	V_{DD}=15V, I_D=-1A, V_{GS}=-10V, R_G=6Ω		4.6	9	ns
t_r	Rise Time[2,3]			14	26	
$t_{d(off)}$	Turn-Off Time[2,3]			34	58	
t_f	Fall Time[2,3]			18	35	

Note :

2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

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Typical Performance Characteristics

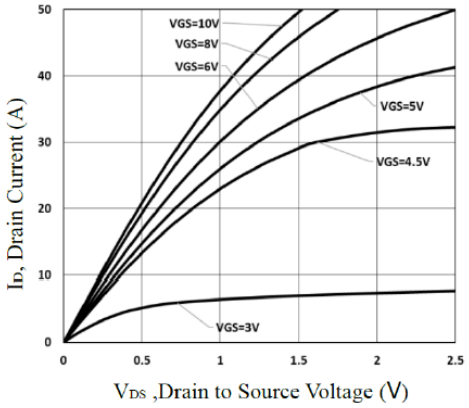

Fig.1 Typical Output Characteristics

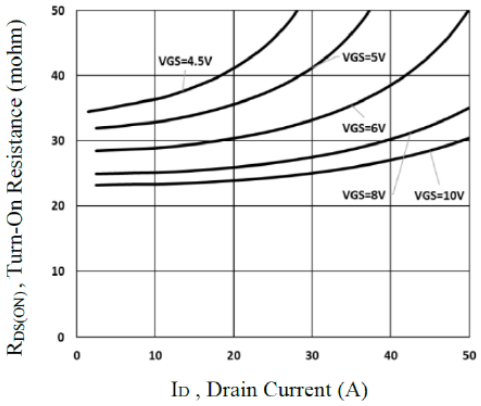

Fig.2 Turn-On Resistance vs I_D

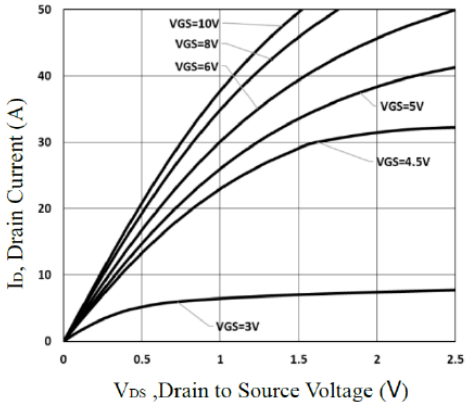

Fig.3 Continuous Drain Current vs T_C

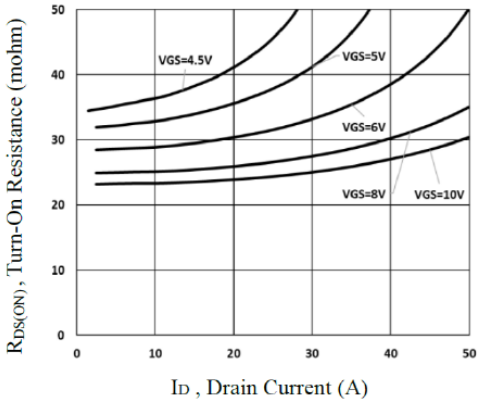

Fig.4 Normalized R_{DSON} vs T_J

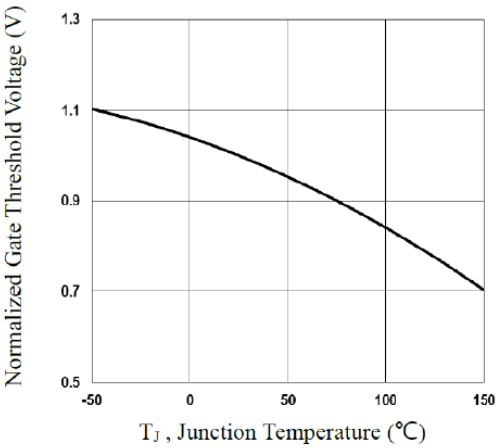

Fig.5 Normalized Vth vs T_J

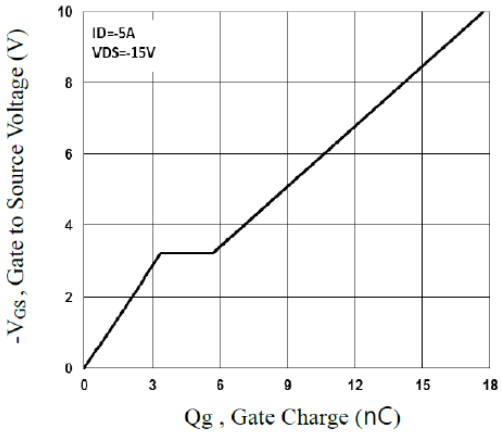

Fig.6 Gate Charge Characteristics

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Typical Performance Characteristics(continue)

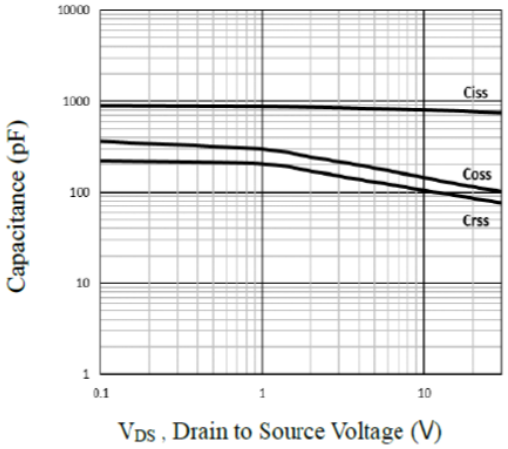

Fig.7 Capacitance Characteristics

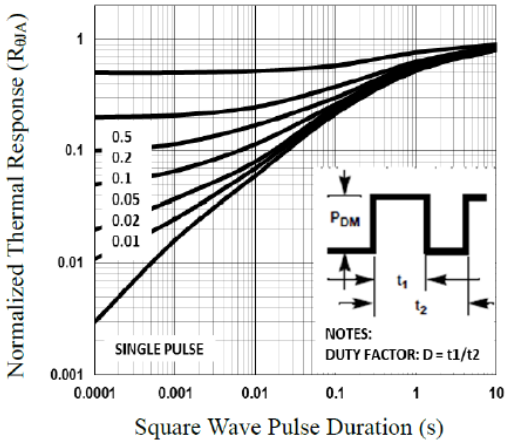

Fig.8 Normalized Transient Impedance

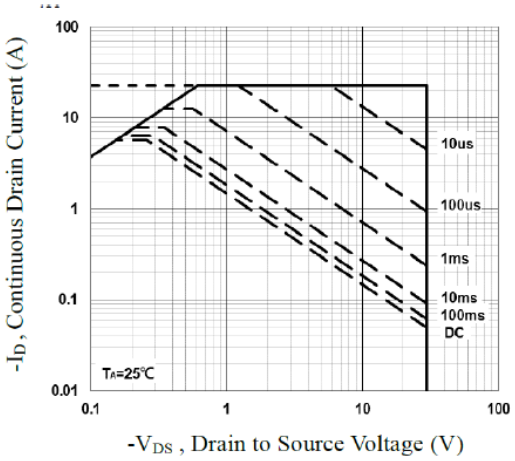

Fig.9 Maximum Safe Operation Area

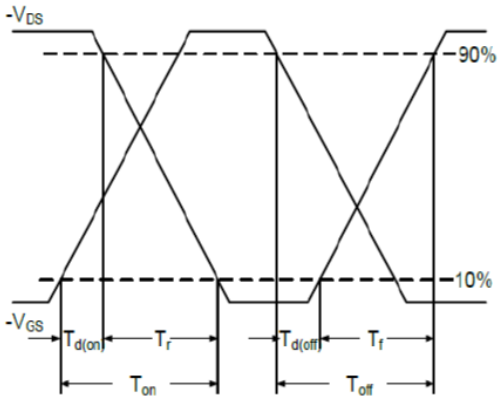

Fig.10 Switching Time Waveform

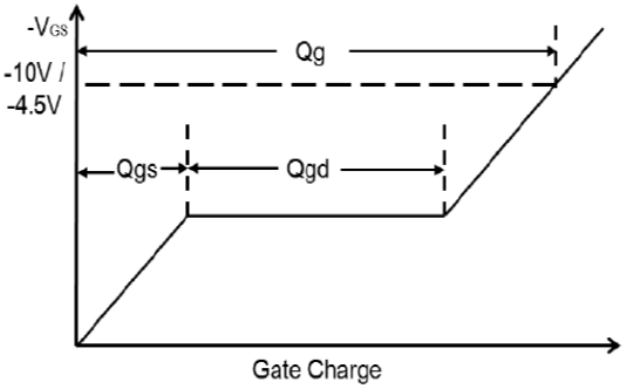

Fig.11 Gate Charge Waveform

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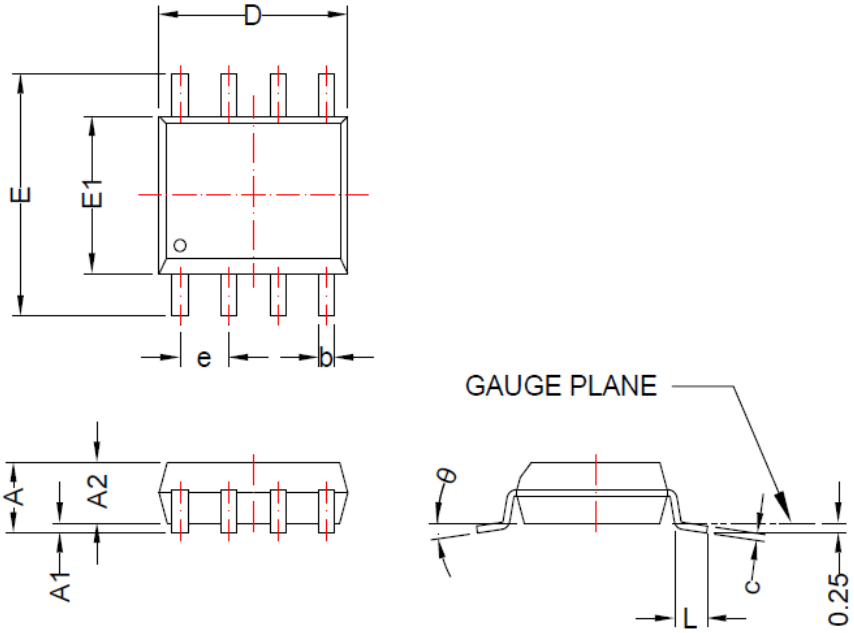
Package Dimension:

SOP-8



DIMENSION D DOES NOT INCLUDE MOLD FLASH,PROTRUSIONS OR GATE BURRS.MOLD FLASH,PROTRUSIONS OR GATE BURRS SHALL HOT EXCEED 0.25mm PER INTERLEAD FLASH OR PROTRUSIOB SHALL NOT EXCEED 0.25mm PER SIDE.

Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	---	1.75	---	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	---	0.049	---
b	0.31	0.51	0.012	0.020
c	0.10	0.25	0.004	0.010
D	4.70	5.10	0.185	0.201
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.4	1.27	0.016	0.050
θ	0°	8°	0°	8°

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