LMP3117SF 30V P-Channel MOSFET

Features

- -30V/-13.8A, $R_{DS(ON)}$<18mΩ@V_{GS}=-10V
- Fast switching
- Suit for -4.5V Gate Drive Applications
- Green Device Available
- SOP-8 package design

Product Description

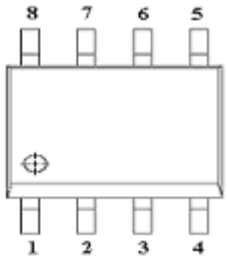
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
These devices are well suited for high efficiency fast switching applications..

Applications

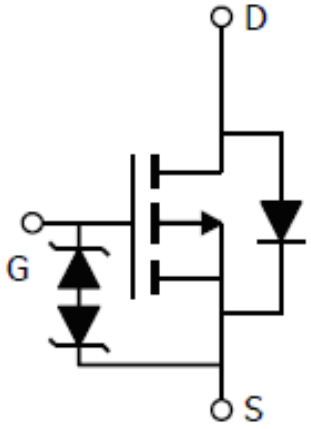
- MB / VGA / Vcore
- POL Applications
- Load Switch
- LED Application

Pin Configuration

LMP3117SF (SOP-8)



PIN	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3117SF	LMP3117	S	F	SOP-8	4000

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
3117SF XWMMMM	3117SF	XWMMMM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±25	V
I_D	Continuous Drain Current	T_C=25℃	-13.8	A
		T_C=70℃	-11.1	
		T_A=25℃	-7.8	
		T_A=70℃	-6.2	
I_{DM}	Pulsed Drain Current		-50	A
P_D	Power Dissipation	T_C=25℃	5.3	W
		T_C=70℃	3.4	
		T_A=25℃	1.7	
		T_A=70℃	1.1	
T_J	Operating Junction Temperature Range		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		75	℃/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		24	℃/W

Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.2		-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-30V, V_{GS}=0V			-1	uA
V_{SD}	Diode Forward Voltage[3]	V_{GS}=0V, I_S=-1A			-1	V
$R_{DS(on)}$	Drain-Source On-Resistance[3]	V_{GS}=-10V, I_D=-10A		12.3	18	mΩ
		V_{GS}=-4.5V, I_D=-6A		19.4	26	
Gate charge characteristics						
Q_g	Total Gate Charge[3,4]	V_{DD}=-15V, V_{GS}=-4.5V, I_D=-15A		22		nC
Q_{gs}	Gate-Source Charge[3,4]			8.7		
Q_{gd}	Gate-Drain Charge[3,4]			7.2		
Dynamic characteristics						
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1.0MHz		2215		pF
C_{oss}	Output Capacitance			310		
C_{rss}	Reverse Transfer Capacitance			237		
$t_{d(on)}$	Turn-On Time	V_{DD}=-15V, V_{GS}=-10V, Rg=3.3Ω, I_D=-15A		8		ns
t_r	Rise Time			73.7		
$t_{d(off)}$	Turn-Off Time			61.8		
t_f	Fall Time			24.4		

Typical Performance Characteristics

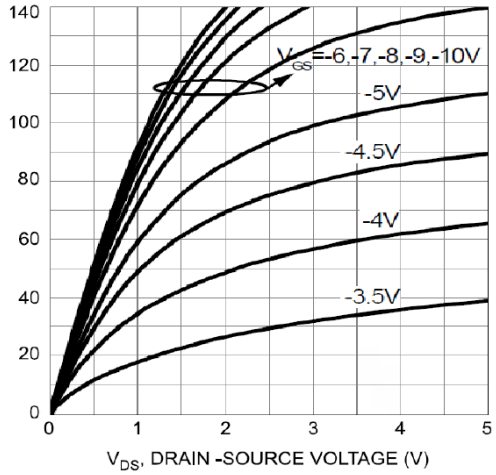


Figure 1. Output Characteristics

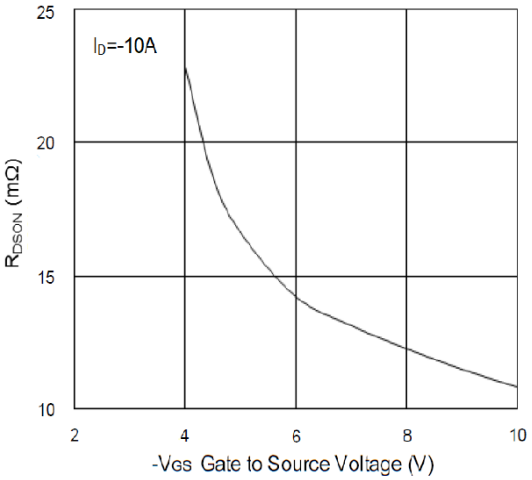


Figure 2. On-Resistance Variation with V_{GS}

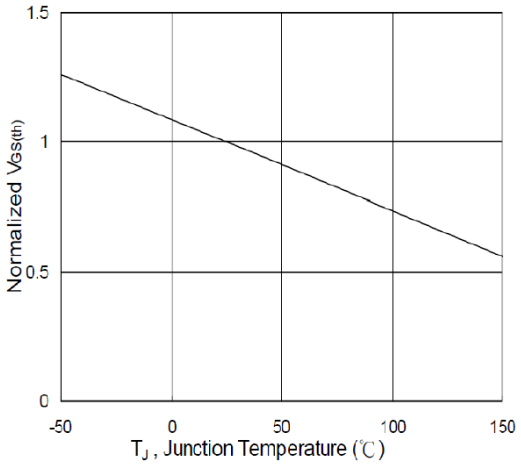


Figure 3. Normalized $V_{GS(th)}$ vs. T_J

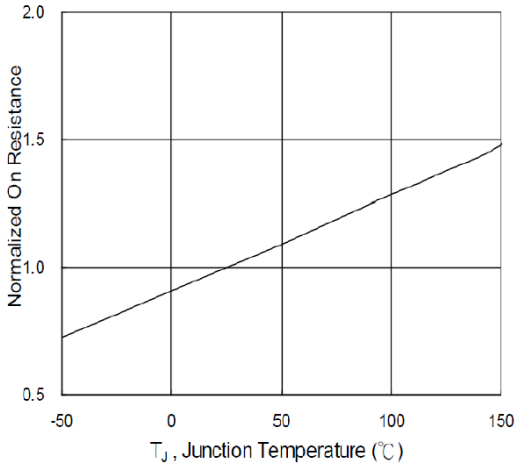


Figure 4. Normalized R_{DSON} vs. T_J

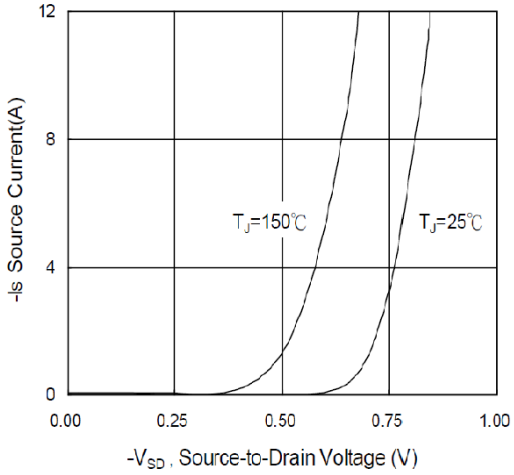


Figure 5. Diode Forward Voltage vs. Current

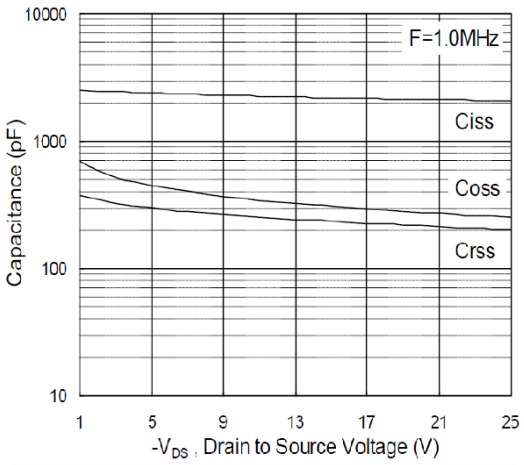


Figure 6. Capacitance

Typical Performance Characteristics(continue)

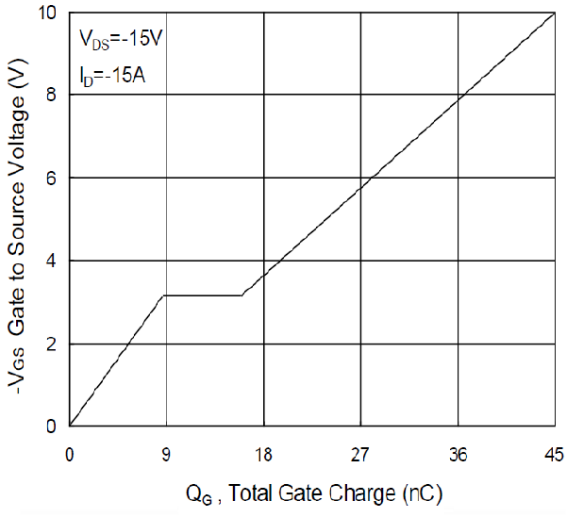


Figure 7. Gate Charge Waveform

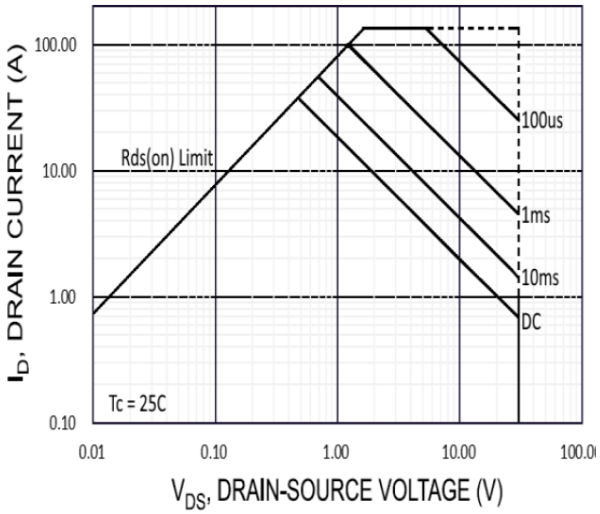


Figure 8. Maximum Safe Operating Area

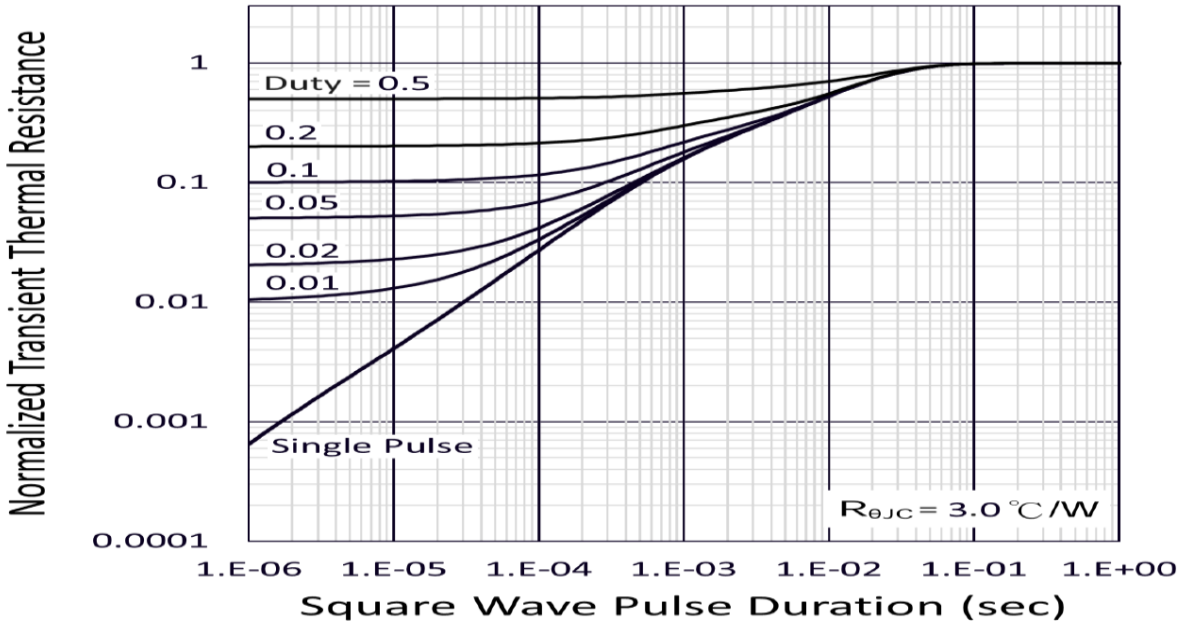
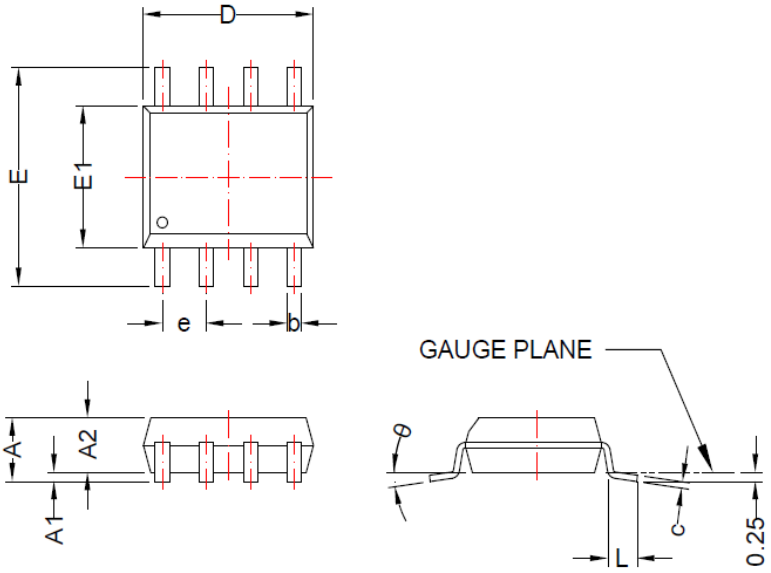


Figure 9. Normalized Transient Thermal Resistance

Package Dimension:

SOP-8



DIMENSI0N D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.
DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE.

Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	---	0.049	---
b	0.31	0.51	0.012	0.020
c	0.10	0.26	0.004	0.010
D	4.70	5.10	0.185	0.201
E	5.80	6.20	0.228	0.244
E1	3.70	4.10	0.146	0.161
e	1.27 BSC		0.050 BSC	
L	0.4	1.27	0.016	0.050
θ	0°	8°	0°	8°

NOTICE:

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