LMP3117ZF 30V P-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)}$=13.5mΩ@V_{GS}=-10V
- Fast switching
- Suit for -4.5V Gate Drive Applications
- Green Device Available
- DFN3X3-8L package design

Product Description

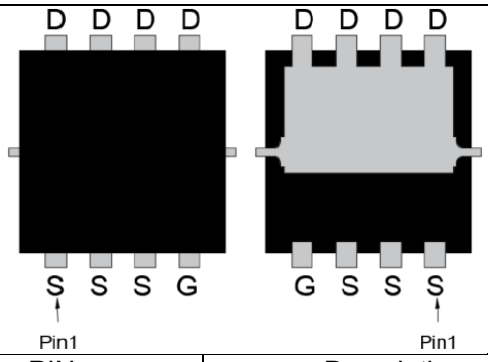
The P-Channel enhancement mode power field effect transistors is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
This device is well suited for high efficiency fast switching applications.

Applications

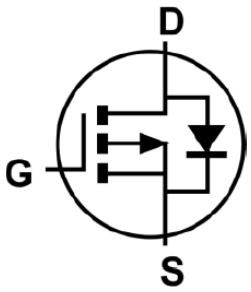
- MB / VGA / Vcore
- POL Applications
- Load Switch
- LED Application

Pin Configuration

LMP3117ZF (DFN3X3-8L)



PIN	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3117ZF	LMP3117	Z	F	DFN3x3-8L	5000pcs

Marking Information

Marking Information	
Product Code	LFC code
3117ZF	□□□□□□

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±25	V
I_D	Continuous Drain Current (T_J=150℃)	T_A=25℃	-31	A
		T_A=100℃	-20	
I_{DM}	Pulsed Drain Current		-70	A
P_D	Power Dissipation	T_A=25℃	22	W
		T_A=100℃	9	
T_J	Operating Junction Temperature		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JC}$	Thermal Resistance Junction to ambient		5.8	℃/W

Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.2	-1.6	-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-30V, V_{GS}=0V			-1	uA
V_{SD}	Diode Forward Voltage[3]	I_S=-1A, V_{GS}=0V			-1	V
$R_{DS(on)}$	Drain-Source On-Resistance[3]	V_{GS}=-10V, I_D=-10A		10.8	13.5	mΩ
		V_{GS}=-4.5V, I_D=-6A		17	25	
Gate charge characteristics						
Q_g	Total Gate Charge[3,4]	V_{DD}=-15V, V_{GS}=-4.5V, I_D=-15A		22		nC
Q_{gs}	Gate-Source Charge[3,4]			8.7		
Q_{gd}	Gate-Drain Charge[3,4]			7.2		
Dynamic characteristics						
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1.0MHz		2215		pF
C_{oss}	Output Capacitance			310		
C_{rss}	Reverse Transfer Capacitance			237		
$t_{d(on)}$	Turn-On Time	V_{DD}=-15V, V_{GS}=-10V, R_g=3.3Ω, I_D=-15A		8		ns
t_r				73.7		
$t_{d(off)}$	Turn-Off Time			61.8		
t_f				24.4		

Typical Performance Characteristics

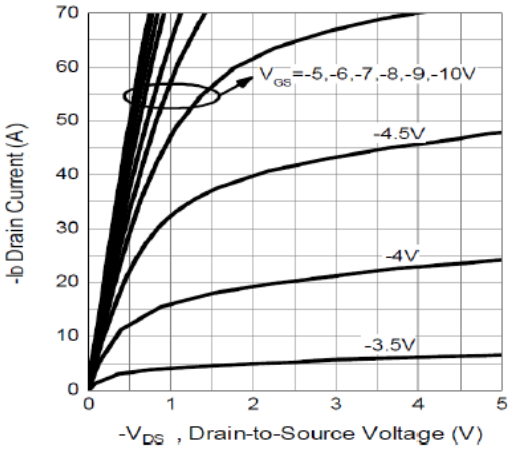


Figure 1. Output Characteristics

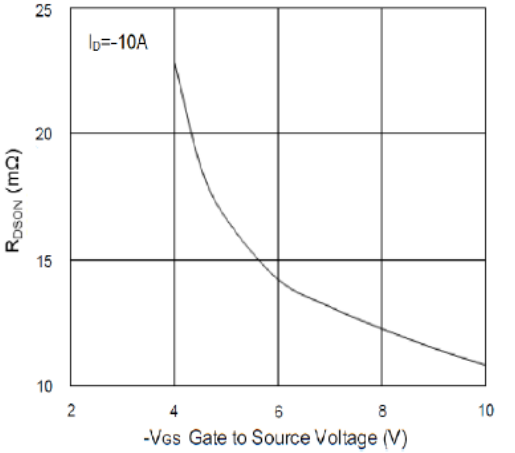


Figure 2. On-Resistance Variation with V_{GS}

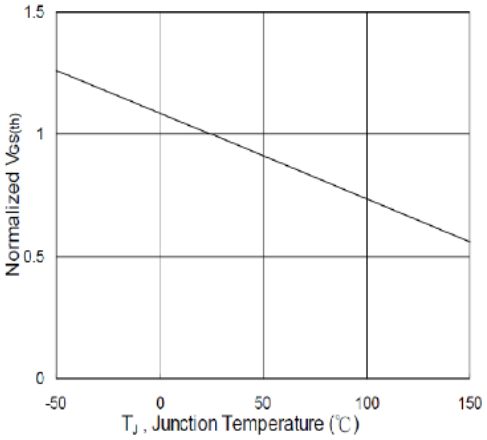


Figure 3. Normalized $V_{GS(th)}$ vs. T_J

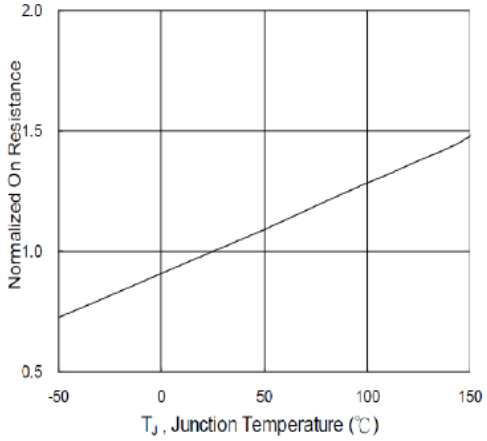


Figure 4. Normalized R_{DSON} vs. T_J

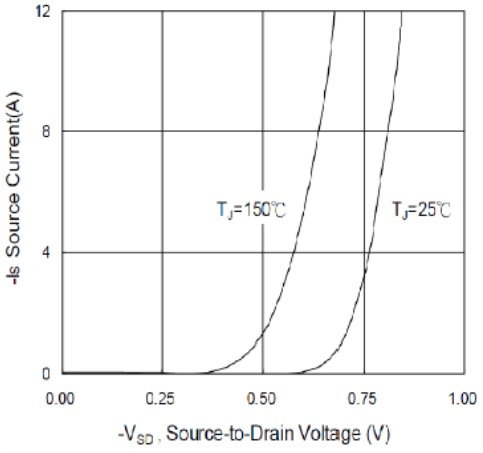


Figure 5. Diode Forward Voltage vs. Current

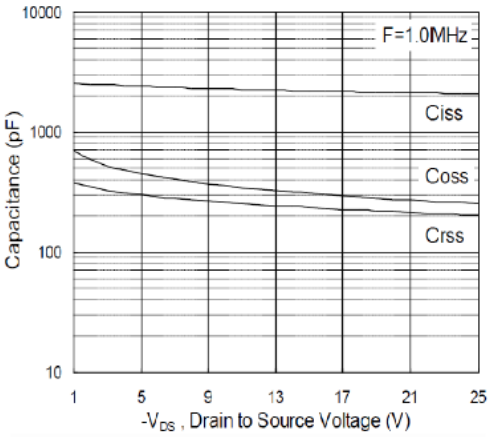


Figure 6. Capacitance

Typical Performance Characteristics(continue)

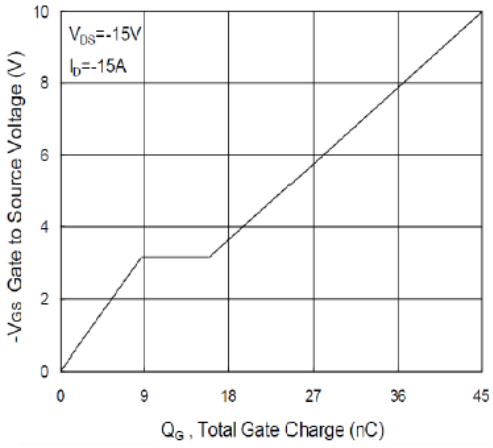


Figure 7. Gate Charge Waveform

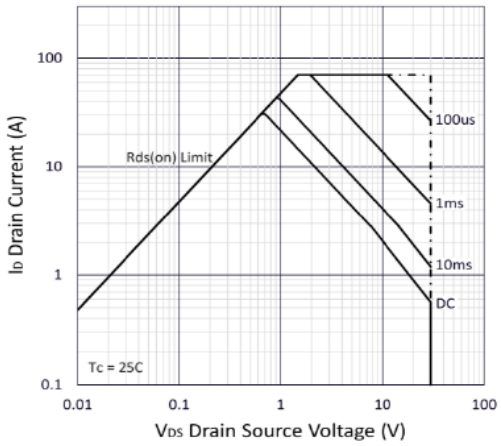


Figure 8. Maximum Safe Operating Area

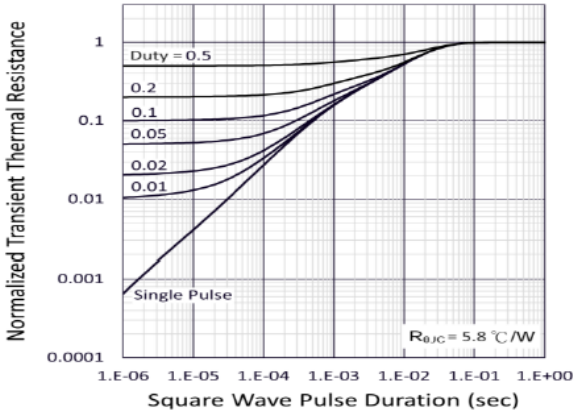
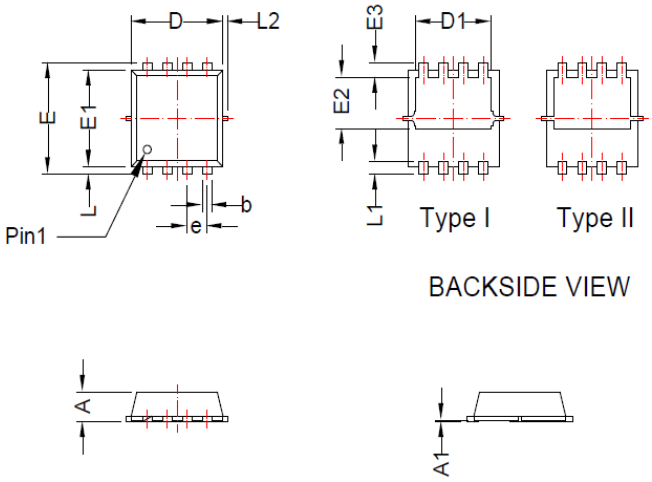


Figure 9. Normalized Transient Thermal Resistance

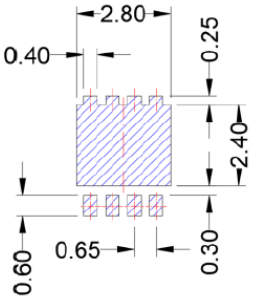
Package Dimension:

DFN3x3-8L

Package Dimension



Recommended Land Pattern



Dimensions				
Symbol	**Millimeters**		**Inches**	
	Min	Max	Min	Max
A	0.70	0.90	0.028	0.035
A1	0.00	0.05	0.000	0.002
b	0.24	0.37	0.009	0.015
c	0.10	0.25	0.004	0.010
D	2.90	3.25	0.114	0.128
D1	2.35	2.60	0.093	0.102
E	3.05	3.45	0.120	0.136
E1	2.90	3.20	0.114	0.126
E2	1.35	2.00	0.053	0.079
E3	0.30	0.60	0.012	0.024
e	0.65 BSC		0.026 BSC	
L	0.02	0.2	0.001	0.008
L1	0.28	0.5	0.011	0.020
L2	-	0.15	-	0.006

NOTE:
Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions

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