LMP1073KTFF 20V P-Channel Enhancement Mode MOSFETs

Features

- -20V/-0.5A, $R_{DS(ON)}$=800mΩ@V_{GS}=-4.5V
- -20V/-0.2A, $R_{DS(ON)}$=1100mΩ@V_{GS}=-2.5V
- -20V/-0.1A, $R_{DS(ON)}$=1800mΩ@V_{GS}=-1.8V
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- ESD Protection
- DFN1006-3L package design

Product Description

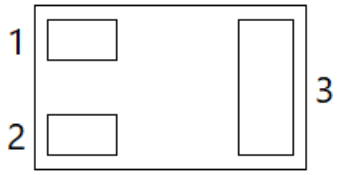
LMP1073KTFF, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent RDS(ON), low gate charge. These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

Applications

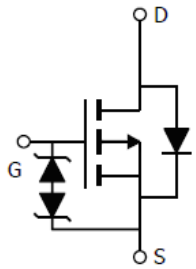
- Drivers , Relays, Solenoids, Lamps, Hammers
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Smart Phones, Pagers

Pin Configuration

LMP1073KTFF (DFN1006-3L)



PIN	Description
1	Gate
2	Source
3	Drain



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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP1073KTFF	LMP1073K	TF	F	DFN1006-3L	-

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
3XWM	3	XWM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Continuous Drain Current (T_J=150℃)	T_A=25℃	-0.47	A
		T_A=70℃	-0.38	
I_{DM}	Pulsed Drain Current		-1.6	A
I_S	Continuous Source Current (Diode Conduction)		-0.3	A
P_D	Power Dissipation	T_A=25℃	0.27	W
		T_A=70℃	0.17	
$R_{\theta JA}$	Thermal Resistance Junction to ambient		463	ºC/W
T_J	Operating Junction Temperature Range		-55 to +150	ºC
T_{STG}	Storage Temperature Range		-55 to +150	ºC

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.3		-1.0	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±10	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V			-1	uA
		V_{DS}=-20V, V_{GS}=0V, T_J=85℃			-30	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-0.5A		545	800	mΩ
		V_{GS}=-2.5V, I_D=-0.2A		760	1100	
		V_{GS}=-1.8V, I_D=-0.1A		980	1800	
g_{FS}	Forward Transconductance	V_{DS}=-10V, I_D=-0.3A		0.8		S
V_{SD}	Diode Forward Voltage	I_S=-0.5A, V_{GS}=0V			-1.3	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=-10V, V_{GS}=-4.5V, I_D=-0.25A		0.62		nC
Q_{gs}	Gate-Source Charge			0.1		
Q_{gd}	Gate-Drain Charge			0.13		
C_{iss}	Input Capacitance	V_{DS}=-16V, V_{GS}=0V f=1MHz		59.8		pF
C_{oss}	Output Capacitance			12.1		
C_{rss}	Reverse Transfer Capacitance			6.4		
$t_{d(on)}$	Turn-On Time	V_{DD}=-10V, R_L=47Ω, I_D≡-0.2A V_{GEN}=-4.5V, R_G=10Ω		5.1		ns
t_r				8.1		
$t_{d(off)}$	Turn-Off Time			28.4		
t_f				20.7		

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Typical Performance Characteristics

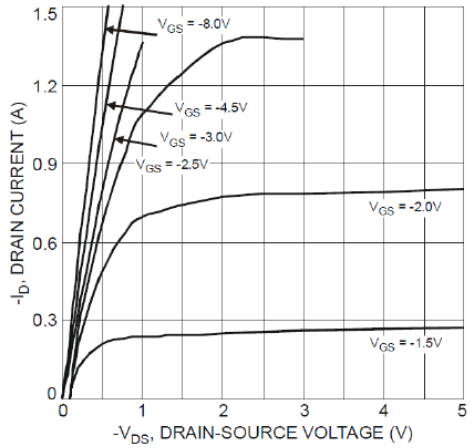

Fig. 1 Typical Output Characteristics

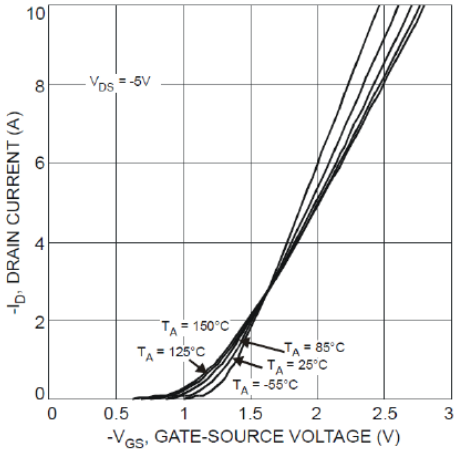

Fig. 2 Typical Transfer Characteristics

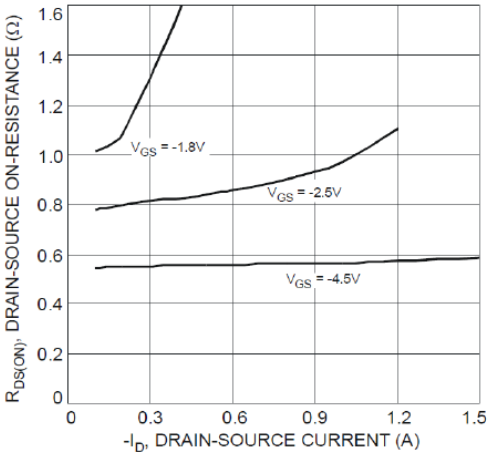

Fig. 3 Typical On-Resistance vs. I_D and V_{GS}

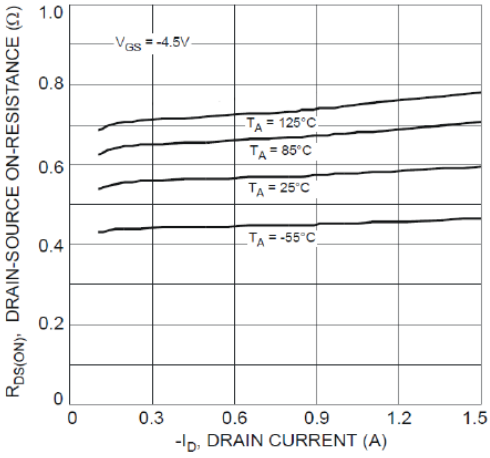

Fig. 4 Typical Drain-Source On-Resistance vs. I_D and T_A

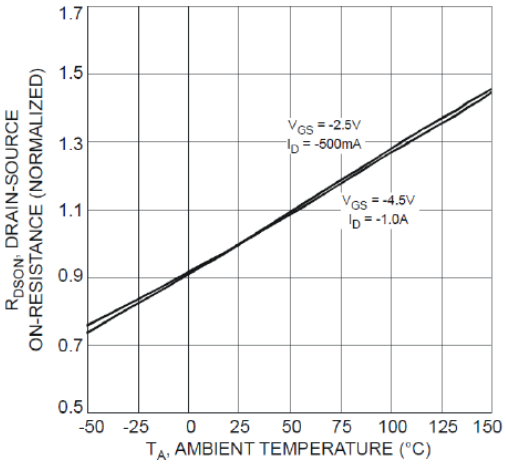

Fig. 5 On-Resistance Variation with T_J

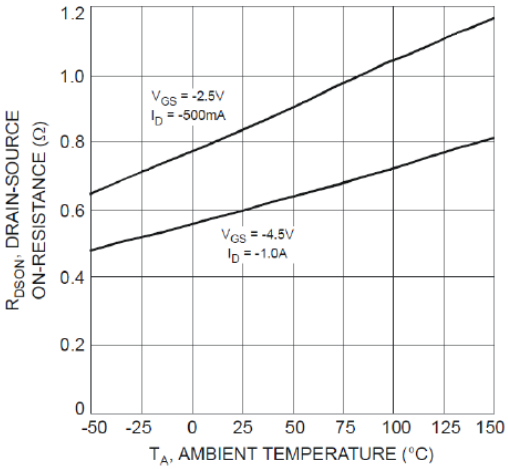

Fig. 6 On-Resistance Variation with T_J

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Typical Performance Characteristics(continue)

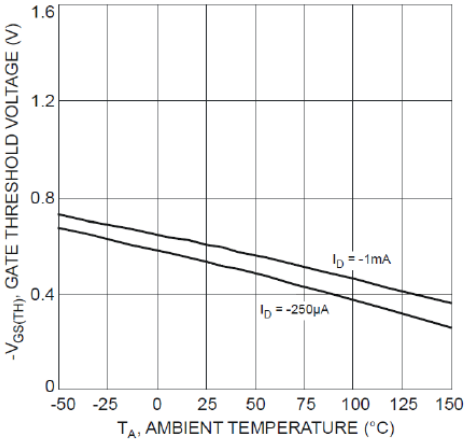

Fig. 7 Gate Threshold Variation vs. T_A

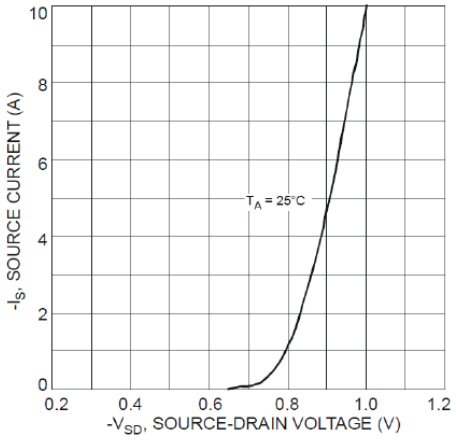

Fig. 8 Diode Forward Voltage vs. Current

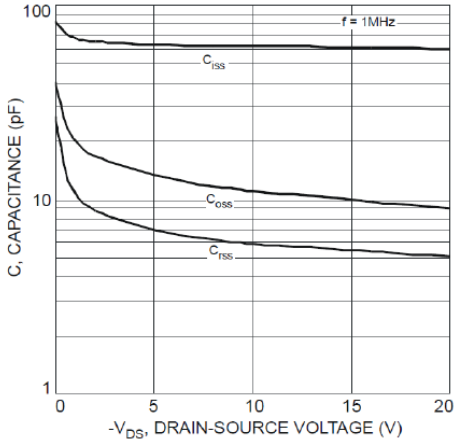

Fig. 9 Typical Capacitance

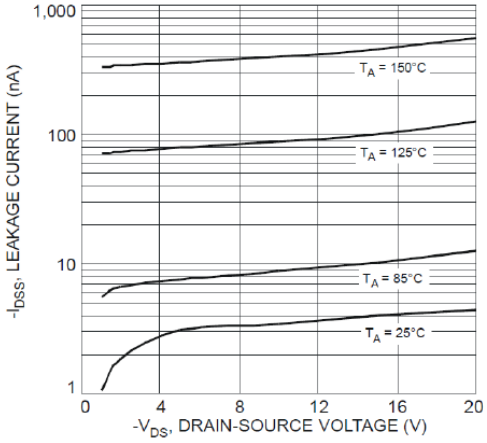

Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

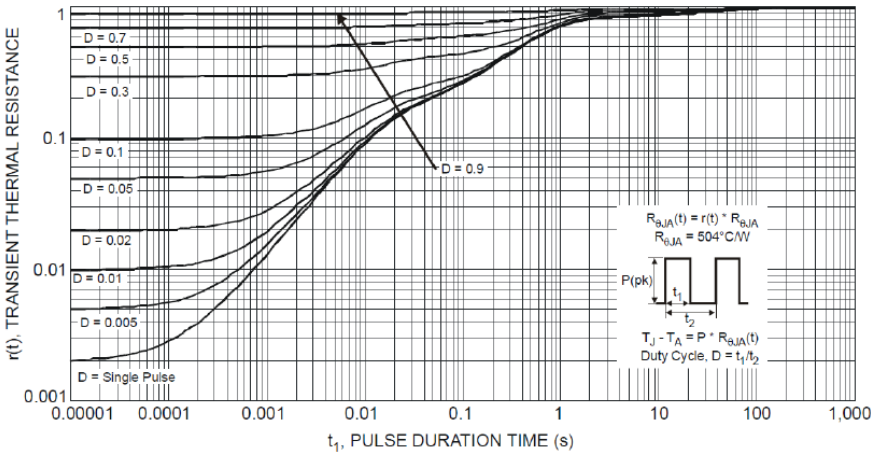

Fig. 11 Transient Thermal Response

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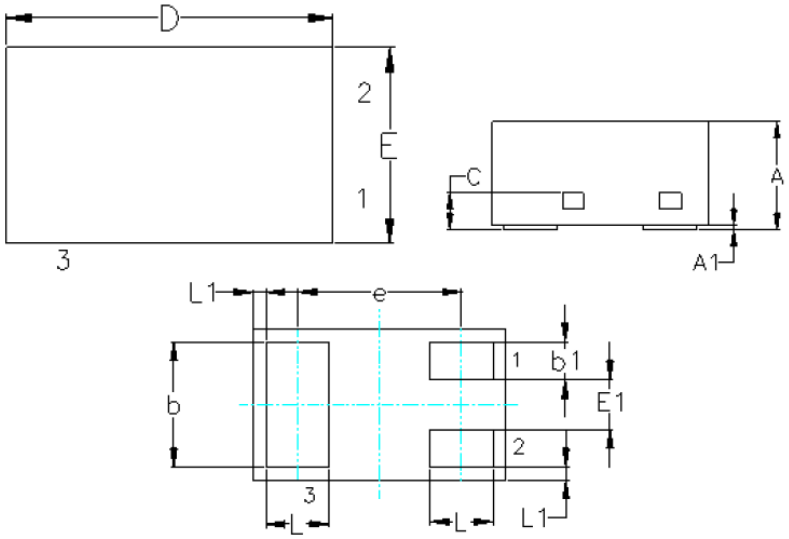
Package Dimension:

DFN1006-3L



Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
b	0.450	0.550	0.018	0.022
b1	0.100	0.200	0.004	0.008
C	0.120	0.180	0.005	0.007
D	0.950	1.050	0.037	0.041
E	0.550	0.650	0.022	0.026
E1	0.150	0.250	0.006	0.010
e	0.650 BSC		0.026 BSC	
L	0.200	0.300	0.008	0.012
L1	0.050 REF		0.002 REF	

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