

## LMP2145X5F 20V P-Channel Enhancement MOSFET

### Features

- -20V/-4A,  $R_{DS(ON)} = 55m\Omega @ V_{GS} = -4.5V$
- -20V/-3A,  $R_{DS(ON)} = 75m\Omega @ V_{GS} = -2.5V$
- -20V/-2A,  $R_{DS(ON)} = 100m\Omega @ V_{GS} = -1.8V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

These devices are particularly suited for low Voltage power management, such as smart Phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

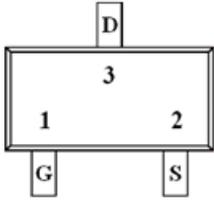
### Product Description

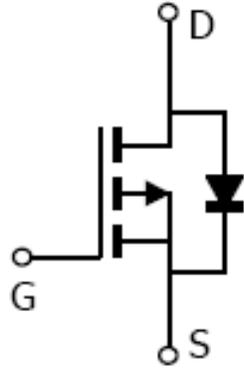
LMP2145, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low gate charge.

### Applications

- Portable Equipment
- Battery Powered System
- Net Working System

### Pin Configuration

LMP2145X5F (SOT-323)	
 <p style="text-align: center;">Top Views</p>	
Pin	Description
1	Gate
2	Source
3	Drain



**Ordering Information**

Part Number	P/N	PKG Code	Pb Free Code	Package	Quantity Reel
LMP2145X5F	LMP2145	X5	F	SOT-323	3000 pcs

**Marking Information**

Part Marking	Part Number	LFC code
45 XW	45	XW

**Absolute Maximum Ratings**

 ( $T_A=25^\circ\text{C}$  Unless otherwise noted)

Symbol	Parameter	Typical	Unit
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>2</sup> (Steady State)	$T_A=25^\circ\text{C}$	-2.3
		$T_A=70^\circ\text{C}$	-1.9
$I_{DM}$	Pulsed Drain Current	-10	A
$P_D$	Power Dissipation ( $T_A=25^\circ\text{C}$ )	0.46	W
$T_J$	Operating Junction Temperature	-55 to +150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient <sup>1</sup>	270	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient <sup>2</sup>	205	$^\circ\text{C/W}$

Note:

1. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

**Electrical Characteristics**

 (T<sub>A</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-20			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-0.4		-0.9	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-16V, V <sub>GS</sub> =0V			-1	uA
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A		49	55	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-3A		66	75	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-2A		90	100	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-3.6A		7.8		S
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =-1.6A		-0.8	-1.2	V
<b>Dynamic</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz		616		pF
C <sub>oss</sub>	Output Capacitance			86		
C <sub>rss</sub>	Reverse Transfer Capacitance			65		
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-10V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-2.3A		6.5		nC
Q <sub>gs</sub>	Gate-Source Charge			1.2		
Q <sub>gd</sub>	Gate-Drain Charge			0.9		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =-10V, I <sub>D</sub> =-1A, V <sub>GS</sub> =-4.5V, R <sub>L</sub> =4Ω, R <sub>G</sub> =6Ω		16		ns
T <sub>r</sub>				27		
t <sub>d(off)</sub>	Turn-Off Time			40		
T <sub>f</sub>				34		

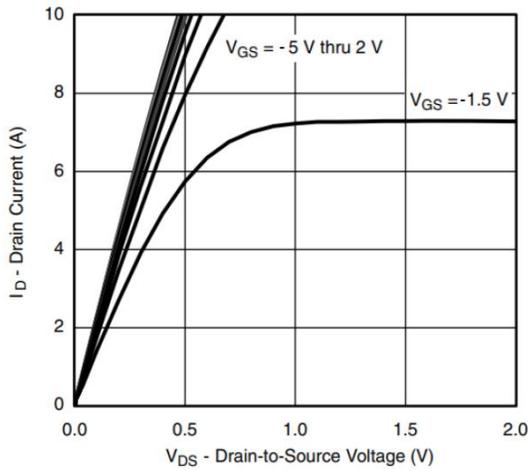
**Typical Performance Characteristics**


Fig.1 Typical Output Characteristics

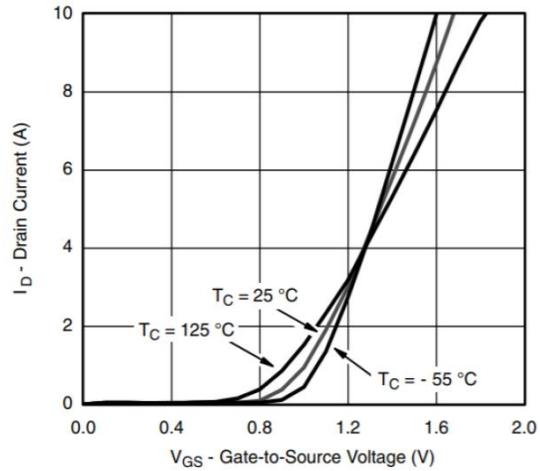


Fig.2 Typical Transfer Characteristics

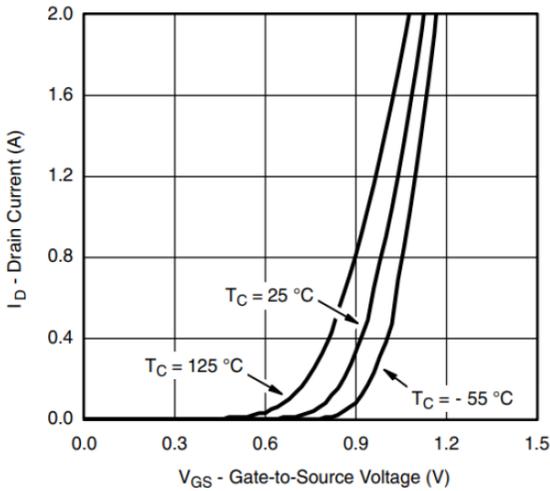
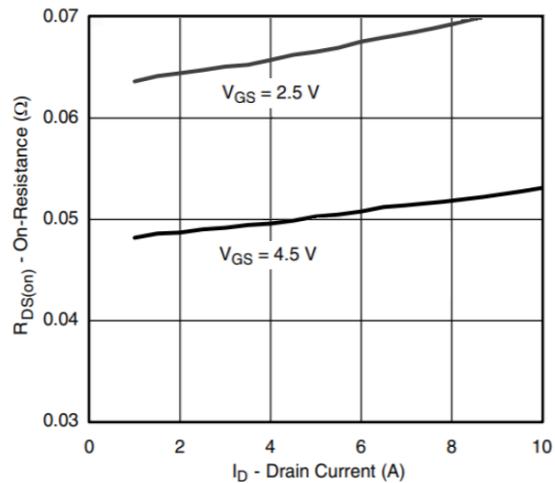
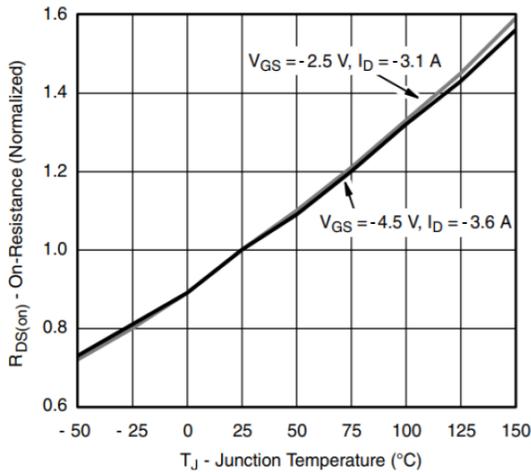
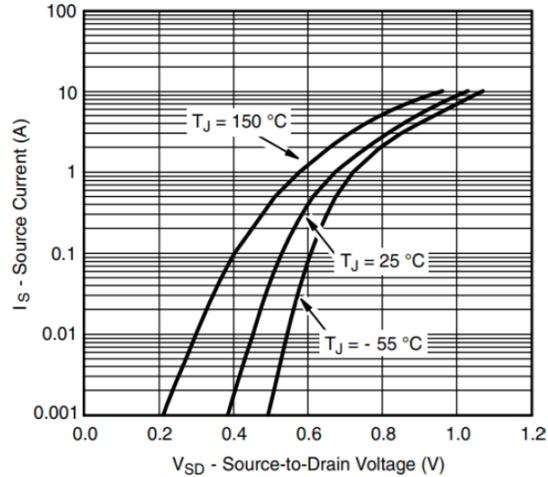
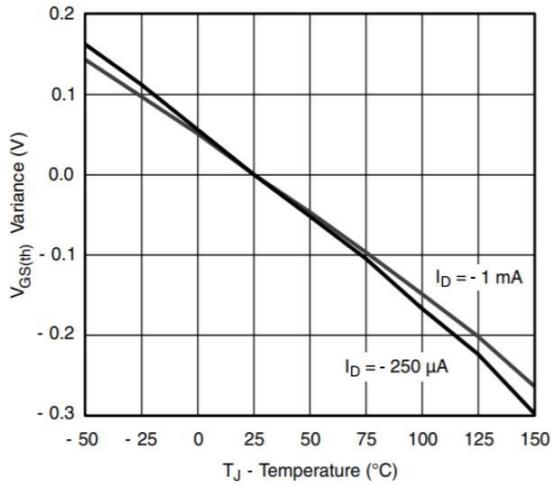
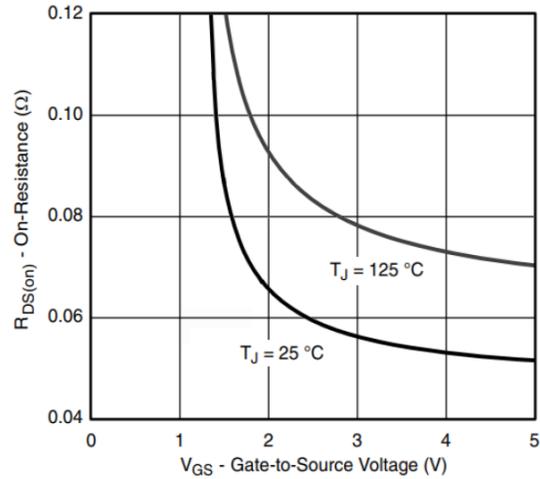
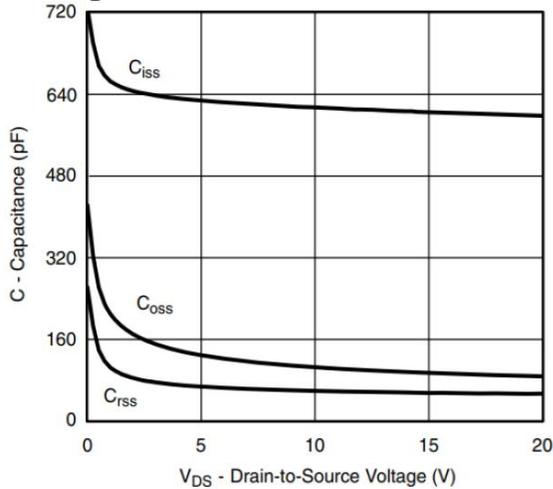
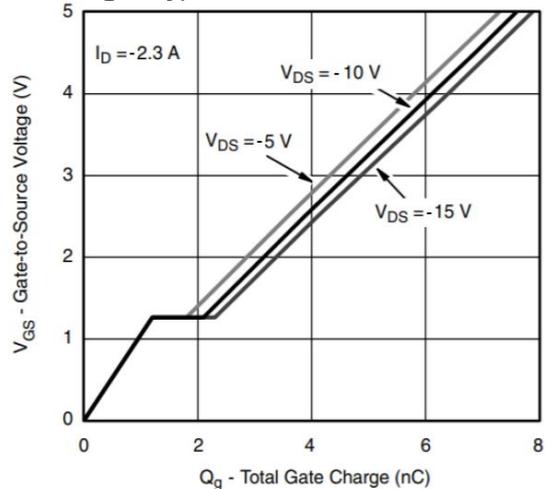
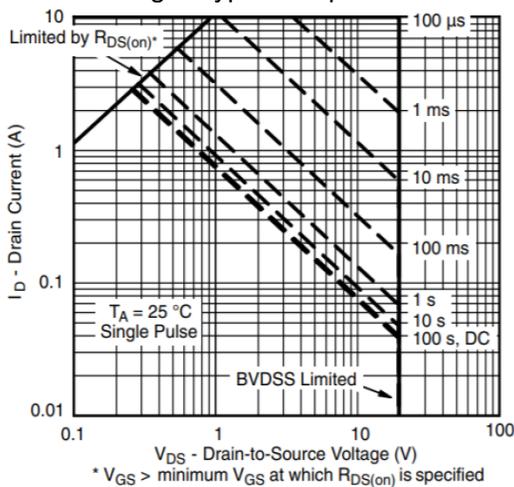
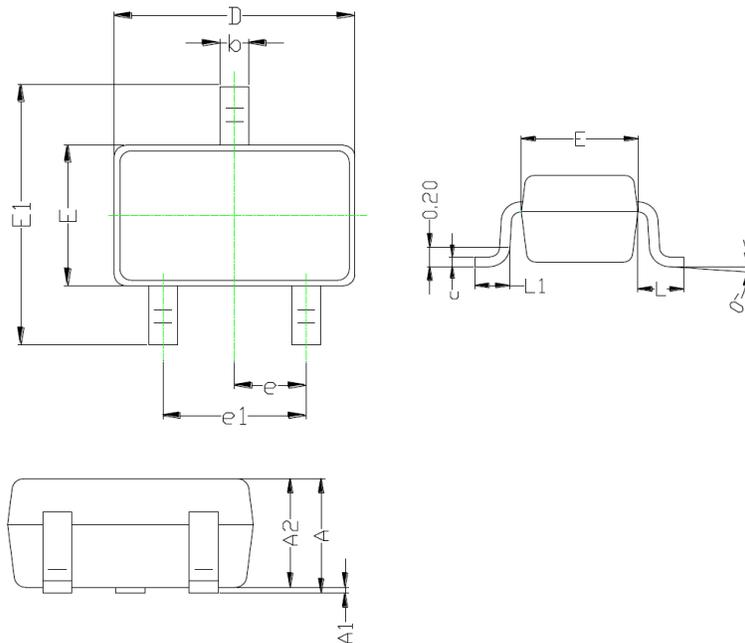

 Fig.3 Typical Drain-Source On-Resistance vs.  $I_D$  and  $T_C$ 

 Fig.4 Typical On-Resistance vs.  $I_D$  and  $V_{GS}$ 

 Fig.5 On-Resistance Variation with  $T_J$ 


Fig.6 Diode Forward Voltage vs. Current

**Typical Performance Characteristics (continue.)**

**Fig.7 Gate Threshold Variation vs.  $T_J$** 

**Fig.8 Typical Transfer Characteristic**

**Fig.9 Typical Capacitance**

**Fig.10 Gate Charge**

**Fig.11 SOA, Safe Operation Area**

**Package Dimension**
**SOT-323**


Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	0.900	1.000	0.035	0.039
<b>A1</b>	0.000	0.100	0.000	0.004
<b>A2</b>	0.900	1.000	0.035	0.039
<b>b</b>	0.200	0.400	0.008	0.015
<b>c</b>	0.080	0.150	0.003	0.006
<b>D</b>	2.000	2.200	0.079	0.086
<b>E</b>	1.150	1.350	0.045	0.053
<b>E1</b>	2.150	2.400	0.084	0.094
<b>e</b>	0.650 TYP		0.025 TYP	
<b>e1</b>	1.200	1.400	0.047	0.055
<b>L</b>	0.525 REF		0.021 REF	
<b>L1</b>	0.260	0.450	0.010	0.017
<b>θ</b>	0°	8°	0°	8°