LMP3415ZF 20V P-Channel Enhancement MOSFET

Features

- $R_{DS(ON)}$ =45mΩ@V_{GS} = -4.5V
- $R_{DS(ON)}$ =58mΩ@V_{GS} = -2.5V
- $R_{DS(ON)}$ =85mΩ@V_{GS} = -1.8V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

These devices are particularly suited for low Voltage power management, such as smart Phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

Product Description

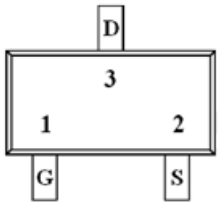
LMP3415ZF, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

Applications

- Portable Equipment
- Battery Powered System
- Net Working System

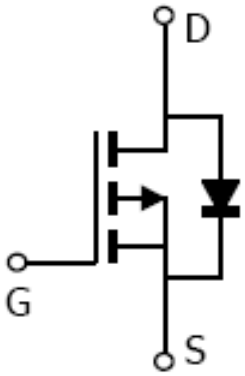
Pin Configuration

LMP3415ZF (SOT-23)



Top Views

Pin	Description
1	Gate
2	Source
3	Drain



Ordering Information

Part Number	P/N	PKG Code	Pb Free Code	Package	Quantity Reel
LMP3415ZF	LMP3415	Z	F	SOT-23	3000 pcs

Marking Information

Part Marking	Part Number	LFC code
15 XW	15	XW

Absolute Maximum Ratings

(T_A=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Continuous Drain Current	T_A=25ºC	-4.9	A
		T_A=70ºC	-3.9	
I_{DM}	Pulsed Drain Current		-10	A
I_S	Continuous Body Diode Forward Current		-1.6	A
P_D	Total Power Dissipation	T_A=25ºC	1.56	W
		T_A=70ºC	1.0	
T_J	Operating Junction Temperature		-55 to +150	ºC
T_{STG}	Storage Temperature Range		-55 to +150	ºC
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		80	ºC/W

Electrical Characteristics

(T_A=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.4		-0.9	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-16V, V_{GS}=0V			-1	uA
		V_{DS}=-16V, V_{GS}=0V, T_J=85ºC			-10	
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-4.9A		40	45	mΩ
		V_{GS}=-2.5V, I_D=-3.4A		50	58	
		V_{GS}=-1.8V, I_D=-2.2A		60	85	
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-3.6A		10		S
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S=-1.6A		-0.85	-1.2	V
Dynamic						
C_{iss}	Input Capacitance	V_{DS}=-10V, V_{GS}=0V, f=1MHz		1050		pF
C_{oss}	Output Capacitance			165		
C_{rss}	Reverse Transfer Capacitance			135		
Q_g	Total Gate Charge	V_{DS}=-10V, V_{GS}=-2.5V, I_D=-4.0A		10	18	nC
Q_{gs}	Gate-Source Charge			2.5		
Q_{gd}	Gate-Drain Charge			3.5		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-10V, I_D=-3.7A, V_{GS}=-4.5V, R_L=2.7Ω, R_G=1Ω		15	25	ns
T_r	Turn-On Rise Time			25	40	
$t_{d(off)}$	Turn-Off Delay Time			40	65	
T_f	Turn-Off Fall Time			15	25	

Typical Performance Characteristics

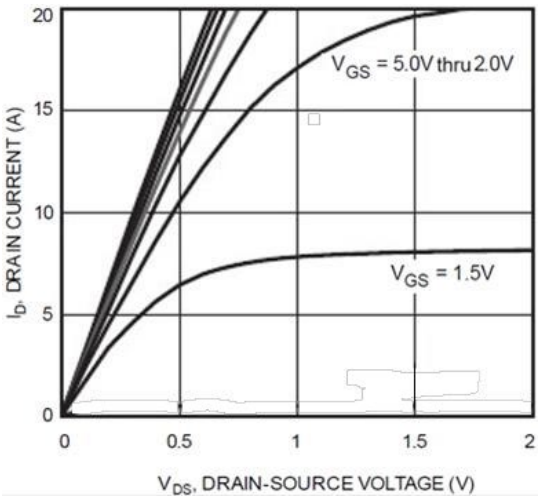


Fig.1 Typical Output Characteristics

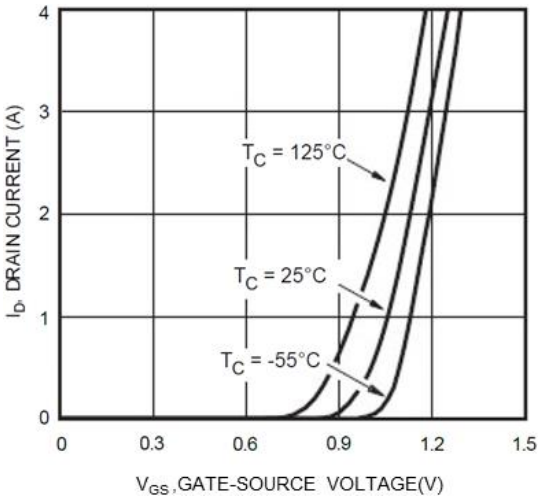


Fig.2 Typical Transfer Characteristics

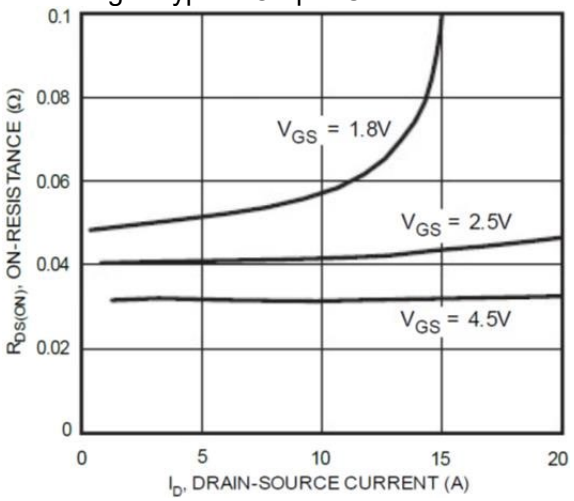


Fig.3 On-Resistance vs. Drain Current

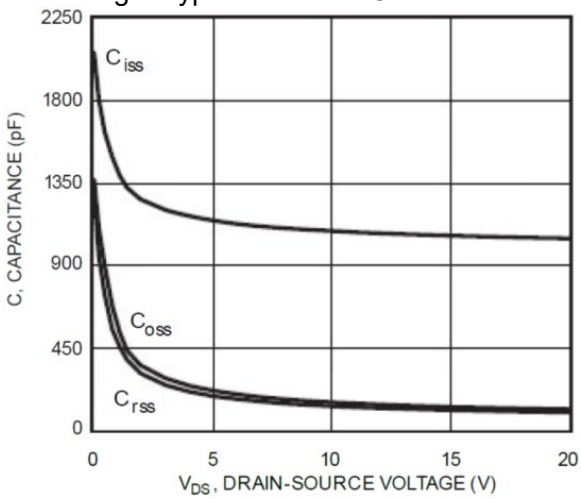


Fig.4 Capacitance vs. Drain-Source Voltage

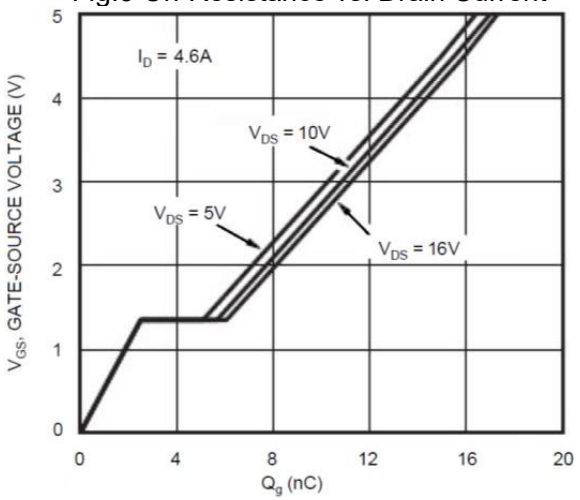


Fig.5 Gate Charge

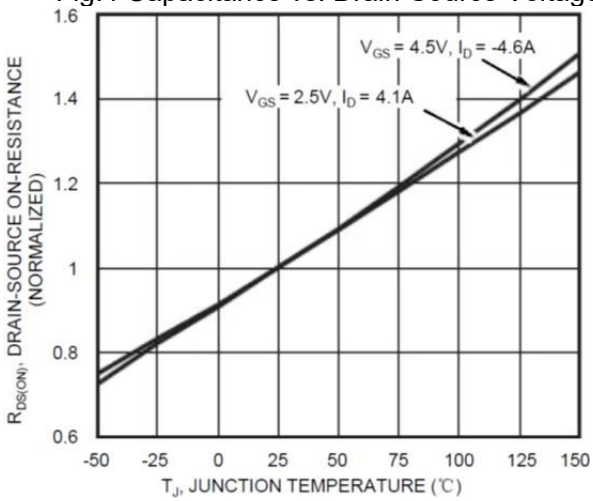


Fig.6 On-Resistance vs. Junction Temperature

Typical Performance Characteristics (continue.)

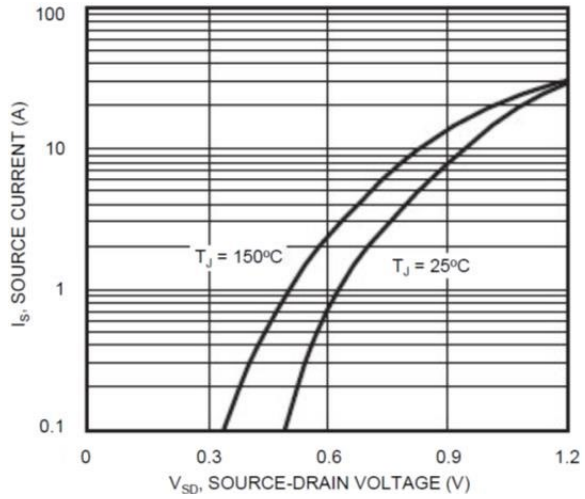


Fig.7 Source-Drain Forward Voltage

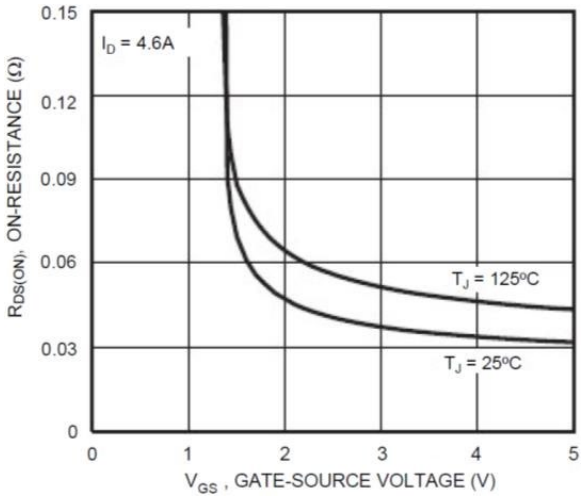


Fig.8 On-Resistance vs. Gate-Source Voltage

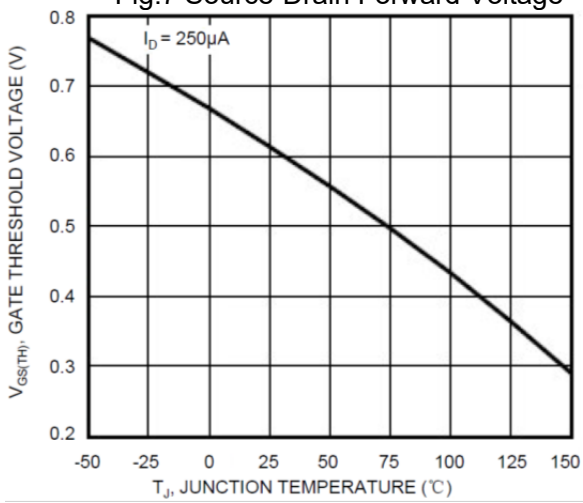


Fig.9 Gate Threshold Voltage vs. Junction Temperature

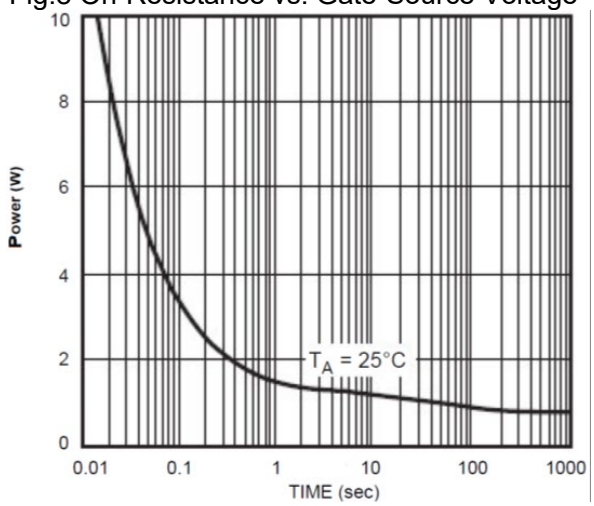


Fig.10 Single Pulse Power

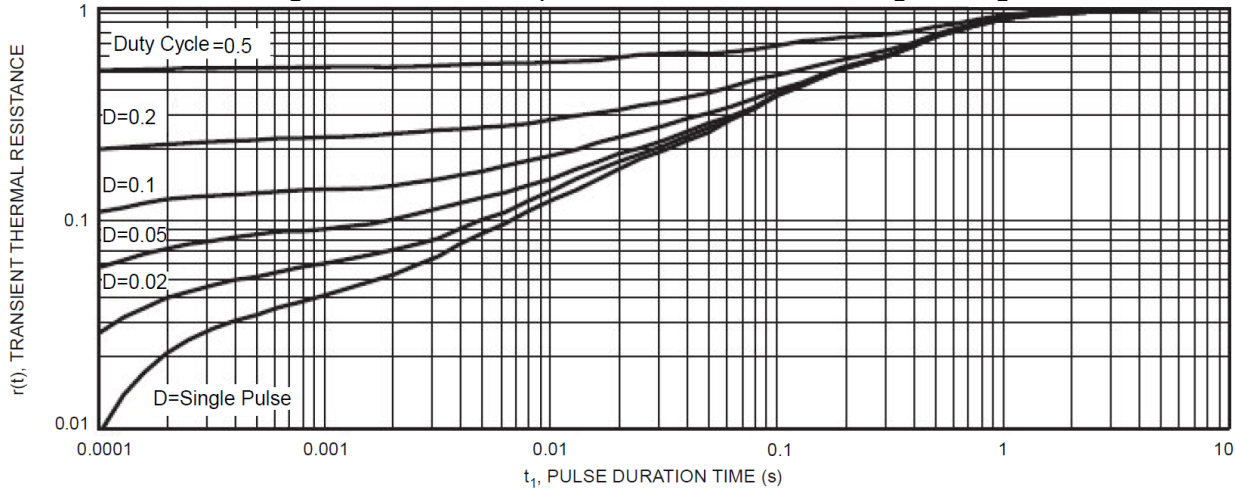
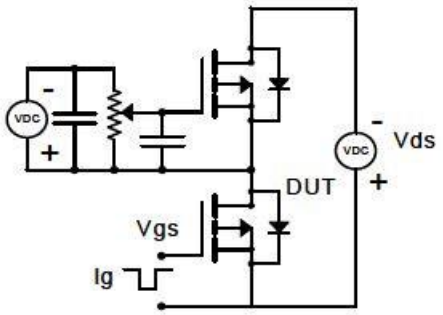
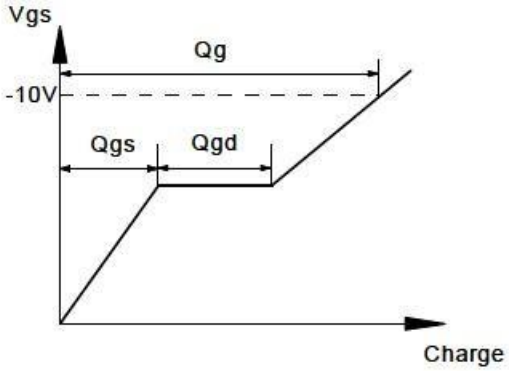


Fig.11 Normalized Thermal Transient Impedance

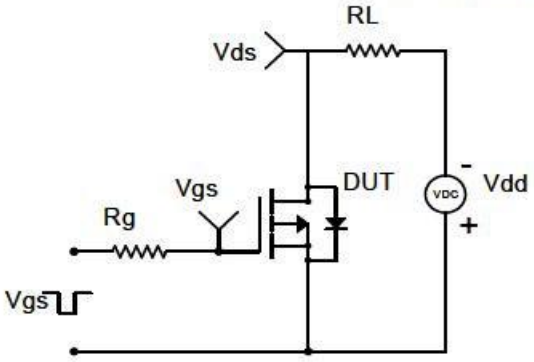
Typical Performance Characteristics (continue.)

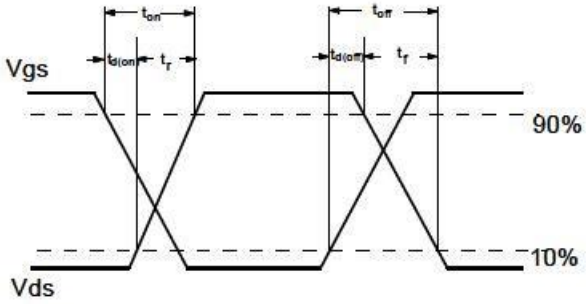
Gate Charge Test Circuit & Waveform



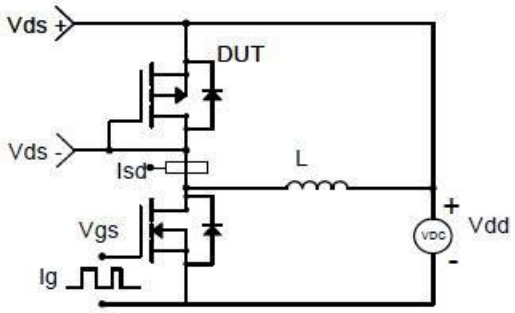


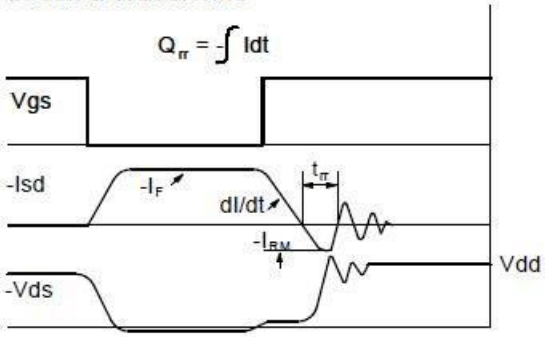
Resistive Switching Test Circuit & Waveforms





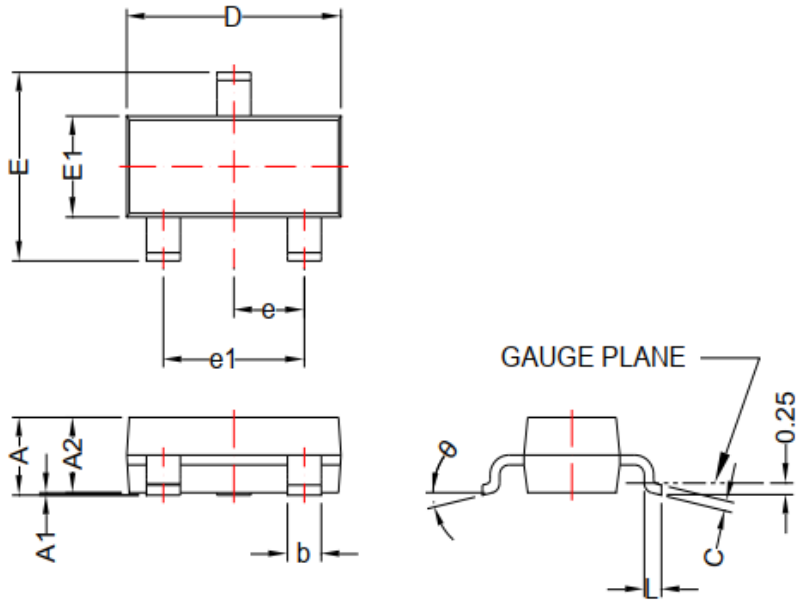
Diode Recovery Test Circuit & Waveforms





Package Dimension

SOT-23



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.750	1.170	0.030	0.046
A1	0.010	0.150	0.000	0.006
A2	0.700	1.020	0.028	0.040
b	0.300	0.500	0.012	0.020
c	0.080	0.200	0.003	0.008
D	2.800	3.040	0.110	0.120
E	2.100	2.640	0.083	0.104
E1	1.200	1.400	0.047	0.055
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°