

LMN22N10SF 100V N-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)} = 22m\Omega @ V_{GS} = 10V$
- $R_{DS(ON)} = 32m\Omega @ V_{GS} = 4.5V$
- Improved dv/dt capability
- Fast switching
- Green Device Available
- SOP-8 package design

Product Description

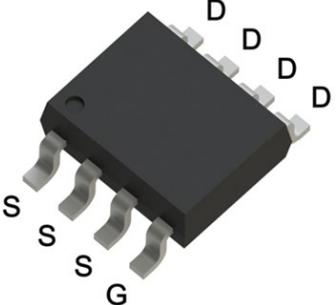
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

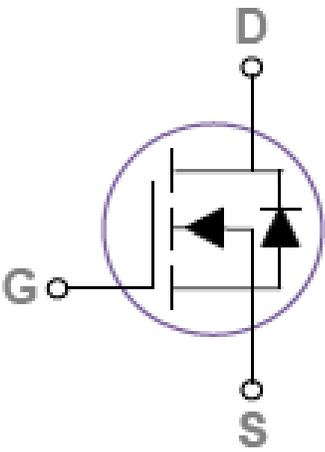
These devices are well suited for high efficiency fast switching applications.

Applications

- Networking
- Load Switch
- LED applications

Pin Configuration

LMN22N10SF (SOP-8)	
	
Pin	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



Ordering Information

Part Number	P/N	PKG Code	Pb Free Code	Package	Quantity Reel
LMN22N10SF	LMN22N10	S	F	SOP-8	4000 pcs

Marking Information

Part Marking	Part Number	LFC code
22N10S XWMMMM	22N10S	XWMMMM

Absolute Maximum Ratings

 ($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V_{DS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current ¹	$T_A=25^{\circ}\text{C}$	7.3
		$T_A=70^{\circ}\text{C}$	5.8
I_{DM}	Pulsed Drain Current ²	12	A
P_D	Total Power Dissipation ³	$T_A=25^{\circ}\text{C}$	2.5
		$T_A=70^{\circ}\text{C}$	1.6
T_J	Operating Junction Temperature Range	-50 to +150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature Range	-50 to +150	$^{\circ}\text{C}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case ¹	50	$^{\circ}\text{C}/\text{W}$

Note:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. The power dissipation is limited by 150°C junction temperature.

Electrical Characteristics

 (T_A=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
B _{VDS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	2	3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V			1	uA
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			7.3	A
I _{SM}	Pulsed Source Current				30	
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =10A		18	22	mΩ
		V _{GS} =6V, I _D =5A		18.7	24	
		V _{GS} =4.5V, I _D =5A		19.6	32	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =3A		14.5		S
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A			1	V
Dynamic						
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		4708		pF
C _{oss}	Output Capacitance			326		
C _{rss}	Reverse Transfer Capacitance			247		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		1.6		Ω
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =10V, I _D =20A		75		nC
Q _{gs}	Gate-Source Charge			15.5		
Q _{gd}	Gate-Drain Charge			20.3		
t _{d(on)}	Turn-On Delay Time	V _{DD} =50V, I _D =1A, V _{GS} =10V, R _G =6Ω		11.5		ns
T _r	Turn-On Rise Time			29		
t _{d(off)}	Turn-Off Delay Time			42		
T _f	Turn-Off Fall Time			18		

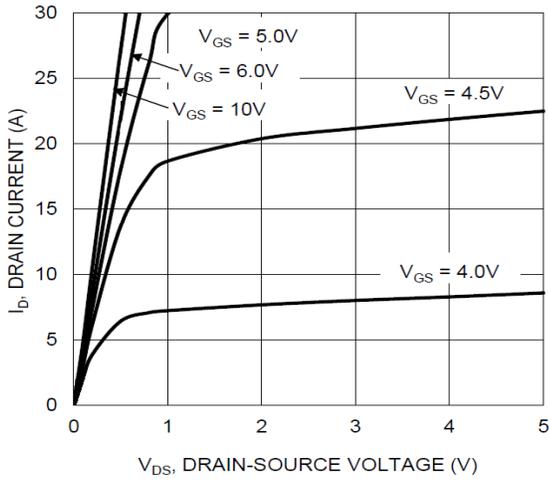
Typical Performance Characteristics


Fig.1 Typical Output Characteristics

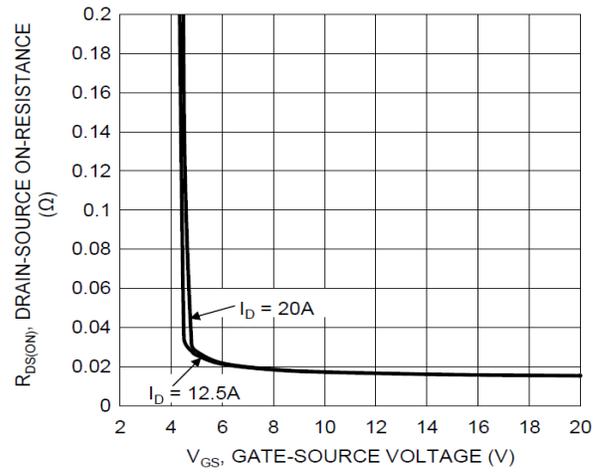


Fig.2 On-Resistance vs. Gate-Source Voltage

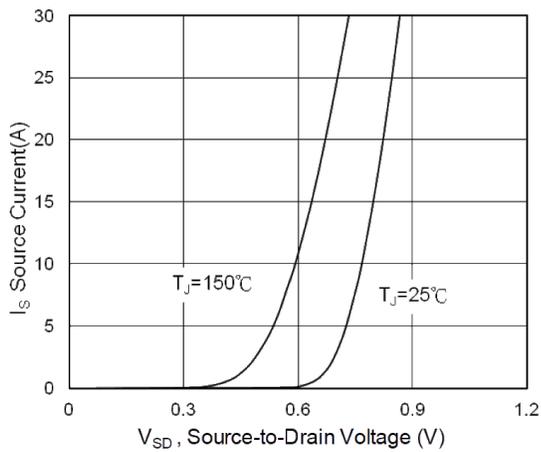


Fig.3 Diode Forward Voltage vs. Current

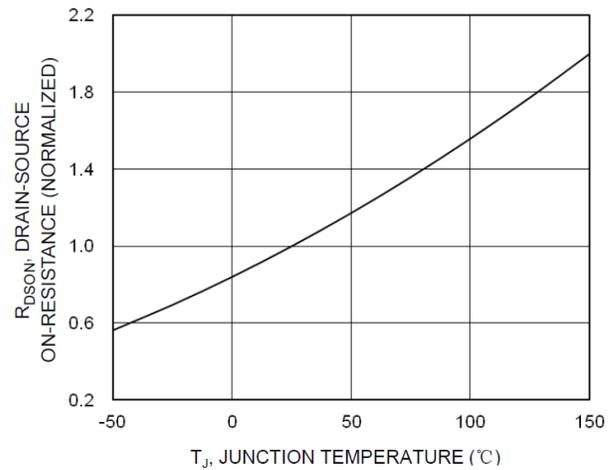
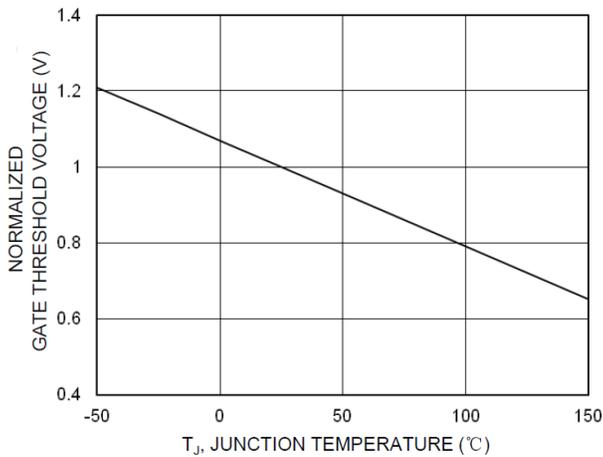
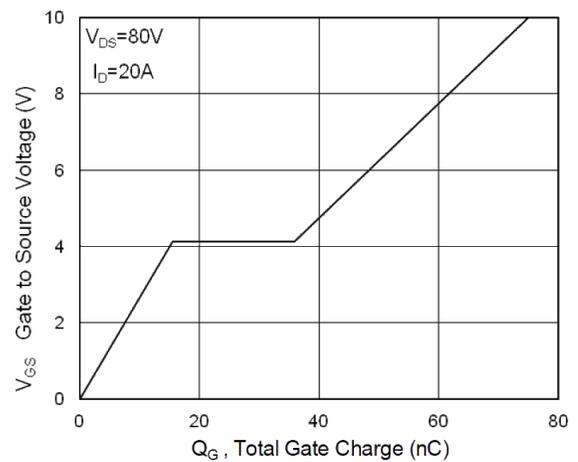

 Fig.4 On-Resistance Variation with T_J

 Fig.5 Gate Threshold Variation vs. T_J


Fig.6 Gate Charge

Typical Performance Characteristics (continue.)

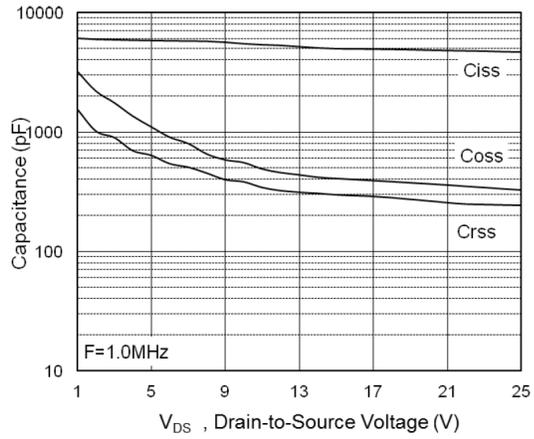
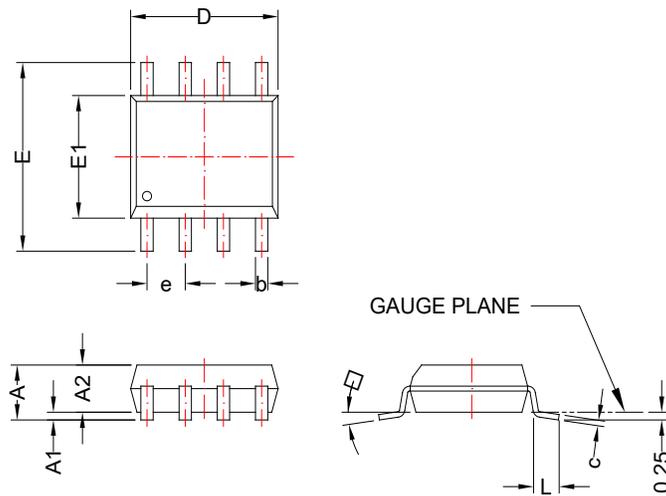


Fig.7 Typical Capacitance

Package Dimension
SOP-8


Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.750	-	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	-	0.049	-
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°