
EMI Reduction Oscillator

Features

- FCC approved method of EMI attenuation
- Proprietary “SaΦic™” technology
- Supply voltage 1.65V~3.63V
- Frequency range 1~125Mhz
- Output Multiple Deviation Selections
- Minimum frequency deviation selection capability
- Pin1 modes: Spread disable
- Package QFN:3.2x2.5mm

Applications

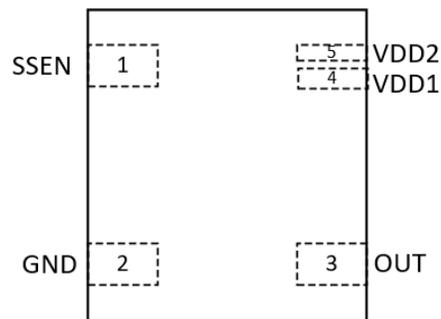
- SATA, Ethernet, PCI express, Video, Wireless
- Computing, Storage, Networking, Telecom, Industrial Control

Table1. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Condition
Output Frequency Range	F	1	100	125	MHz	V _{DD} =1.8V
Frequency Stability	F _{stab}	-20		+20	PPM	Inclusive of initial tolerance at 25 °C, and variations over operating temperature, rated power supply voltage and load.
Operating Temperature Range	T _{use}	-40		+85	°C	
Supply Volage	V _{DD}	1.65	1.8-3.3	3.63	V	
Current Consumption	I _{DD}	-		28	mA	No load condition, f=100MHz, V _{DD} =1.8V
OE mode disable current	I _{od}			18	mA	When OE=GND, output is Pulled Down
Duty Cycle	DC	45		55	%	Please refer figure 2
Rise/Fall Time	T _r , T _f		1.5		nS	15pF load, 10%~90% V _{DD} , high drive (V _{DD} =1.8V)
Output Voltage High	V _{OH}	V _{DD} -0.4	-	-	V _{DD}	I _{OH} =-4mA, I _{OL} =4mA, Standard Drive
Output Voltage Low	V _{OL}	-	-	0.4	V _{DD}	
Input Voltage High	V _{IH}	70%	-	-	V _{DD}	Pin1, OE
Input Volage Low	V _{IL}	-	-	30%	V _{DD}	Pin1, OE
Startup Time	T _{start}	-	5	7	mS	Measure from the time V _{DD} reaches its rated minimum value.
PK-PK Period Jitter	T _{jitt}	-	200	350	pS	F=100MHz, V _{DD} =1.8V
First year Aging	F _{aging}	-1.5		+1.5	PPM	25 °C
10-year Aging		-5		+5	PPM	

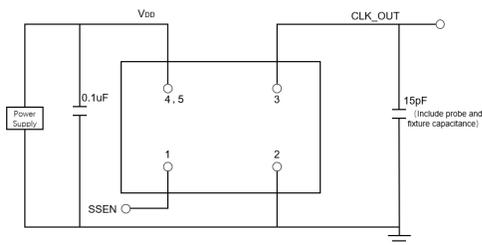
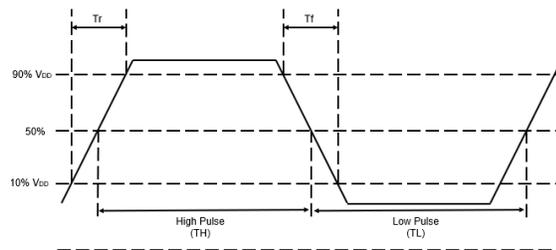
Table2. Pin Configuration

Pin	Symbol		Functionality
1	SSEN	Input	Modulation Output Clock Mode Enable Pin H (Logic "1"): Enable L (Logic "0"): Disable
2	GND	Power	Electrical ground
3	OUT	Output	Oscillator output
4	VDD1	Power	Power supply voltage
5	VDD2	Power	Power supply voltage

TOP View

Table3. Deviation select Table

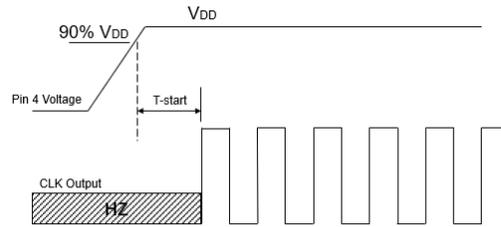
Deviation Select	1	2	3	4
Deviation	-0.9%	±0.45%	-0.5%	±0.25%

Notes: Please refer to ordering information for deviation select.

Test Circuit and Waveform

Figure 1. Test Circuit

Figure 2. Waveform

Notes: Duty Cycle is computed as Duty Cycle = TH/Period.

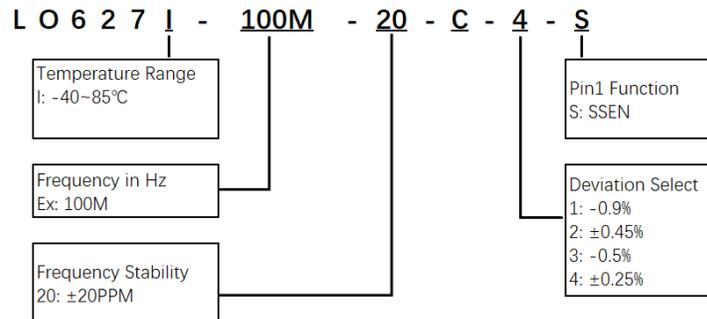
Timing Diagram



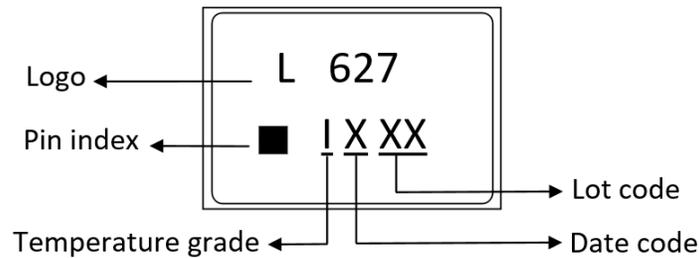
T-start: Time to start from power-off

Figure 3. Startup Timing

Ordering Information

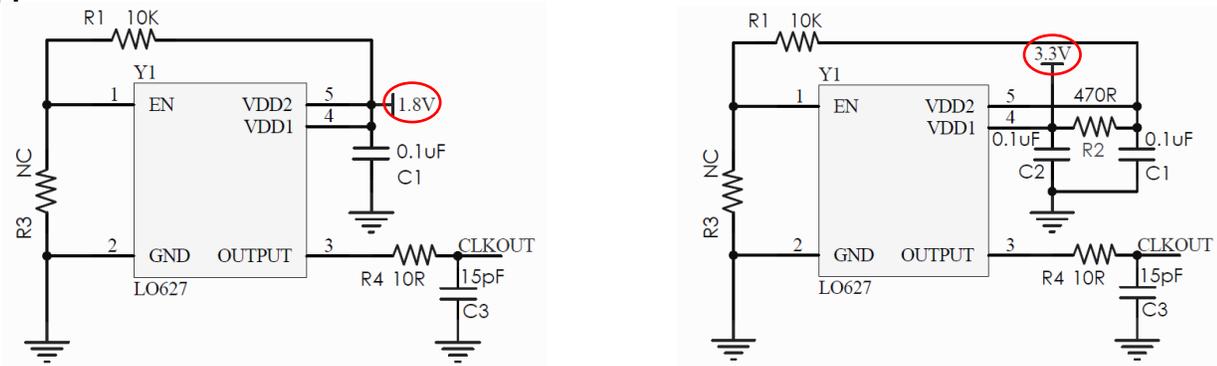


Marking



Temperature Grade	Temperature Range	Frequency Stability (PPM)
I	-40~85°C	±20

Application Schematic



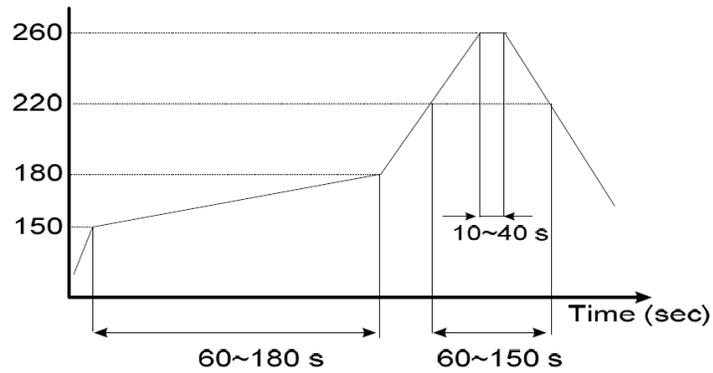
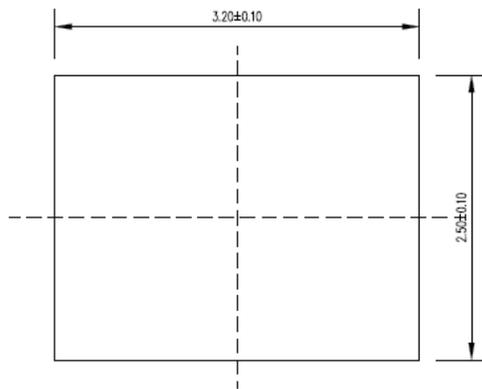
Remark: Footprint please refer page4.

Rev:1.5

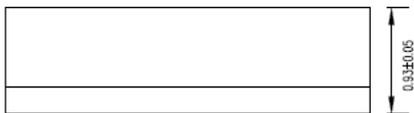
Notice: The information in this document is subject to change without notice.

Suggested reflow profile
Total time :600 sec. Max Solder melting point:220°C

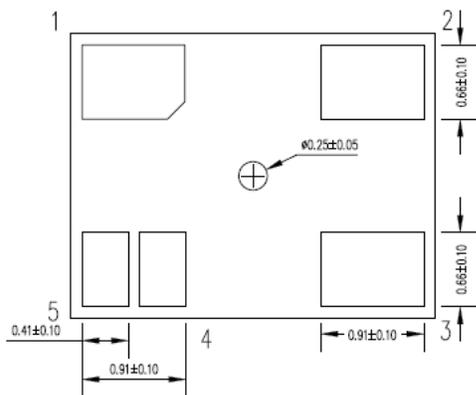
Temp. (°C)


Package Dimension


Top View

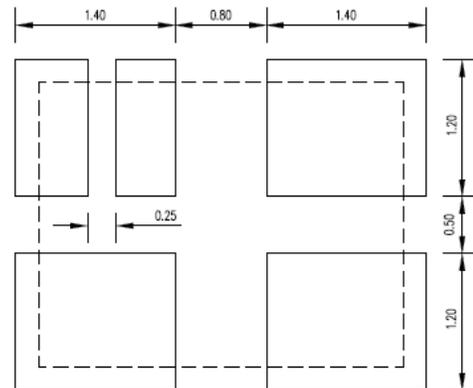


Side View

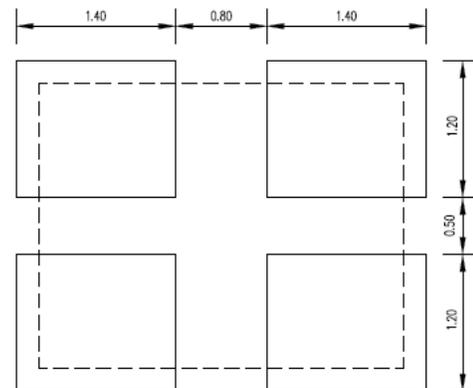


Bottom View

Units : mm



For 3.3V Suggested Layout



For 1.8V Suggested Layout

Revision History

Revision Number	Date of Release	Changes
1.0	12/01/2023	Preliminary datasheet
1.1	03/22/2024	Modify the marking
1.2	12/06/2024	Add 3.3V application.
1.3	01/06/2025	Add -0.5%, -0.9% deviation
1.4	03/25/2025	Updated the pin functionality
1.5	05/23/2025	Modify table3