Low ESR Cap. Compatible Positive Voltage Regulator

Features

- Maximum Output Current: 250mA (4.5V Type)
- Dropout Voltage: 250mV @ 100mA
- Maximum Operating Voltage: 6V
- Output Voltage: 1.2V-5.0V ± 2%
- Low Power Consumption: 1.0μA (TYP.)
- Operating Ambient Temperature: -40℃~ +85℃
- Low ESR Capacitor
- Current Limit Protection
- Available in SOT-23 Package
- ROHS Compliant

Product Description

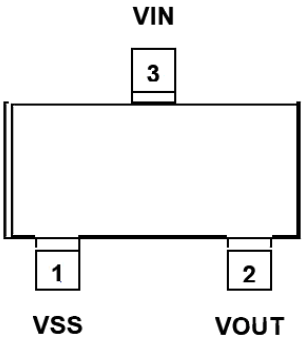
The LPL1206 are highly precise, low power consumption, 3 terminal, positive voltage regulators manufactured using CMOS and laser trimming technologies. The series provides large currents with a significantly small dropout voltage.

The LPL1206 consists of a current limiter circuit, a driver transistor, a precision reference voltage and an error correction circuit. The series is compatible with low ESR ceramic capacitors. The current limiter's foldback circuit operates as a short circuit protection as well as the output current limiter for the output pin.
Output voltages are internally by laser trimming technologies. It is selectable in 0.1V increments within a range of 1.2V to 5.0V in the SOT-23 package.

Applications

- Smart phones / Mobile phones
- Portable game consoles
- Digital still cameras / Camcorders
- Digital audio equipment
- Reference voltage sources
- Multi-function power supplies

Pin Configuration



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Typical Application Circuit

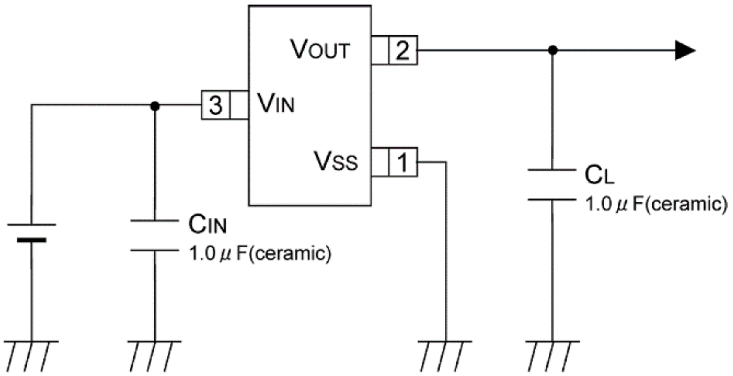

Figure.1 Typical Application Circuit

Pin Function Description

Pin#	Pin Name	Pin Description
1	VSS	Ground.
2	VIN	Power Supply Input. Connecting a 1uF ceramic bypass capacitor between VIN and GND to eliminate noise.
3	VOUT	Regulator output. Connecting a 1uF ceramic bypass capacitor between VOUT and GND.

Absolute Maximum Ratings

Parameter	RATINGS	UNITS
Input Voltage	-0.3～+7.0	V
Output Current	500 (*1)	mA
Output Voltage	-0.3 ~ VIN + 0.3	V
Power Dissipation	250	mW
	500(40mm x 40mm Standard board) (*2)	
Operating Ambient Temperature	- 40 ~ + 85	℃
Storage Temperature	- 55 ~ + 125	℃

(*1) $I_{OUT} \leqq Pd / (VIN-VOUT)$

(*2) The power dissipation figure shown is PCB mounted and is for reference only. The mounting condition is please refer to PACKAGING INFORMATION.

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Electrical Characteristic

(T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions (*1)	Min	Typ	Max	Unit
Output Voltage	$V_{OUT(E)}$ (*2)	I_{OUT}=30mA	x0.98	VOUT (*3)	x1.02	V
Supply Current	I_Q		-	1	3	μA
Load Regulation	Δ_{VOUT}	1mA≦I_{OUT}≦100mA	-	-	60	mV
Dropout Voltage 1	Vdif1(*4)	I_{OUT}=30mA	-	75	350	mV
Dropout Voltage 2	Vdif2(*4)	I_{OUT}=100mA	-	250	680	mV
Line Regulation	ΔV_{OUT}/ (Δ_{VIN}・V_{OUT})	$V_{OUT(T)}$+1V, I_{OUT}=30mA	-	0.05	0.25	%/V
Maximum Output	I_{OUTMAX}	V_{OUT}≧$V_{OUT(E)}$× 0.9	200	-	-	mA
Short Circuit Current	I_{SHORT}	V_{OUT} = V_{GND}	-	100		mA
Input Voltage	V_{IN}		1.8(*5)		6	V
Output Voltage Temperature Characteristics	Δ_{VOUT}/ (ΔTopr*V_{OUT})	I_{OUT}=30mA, -40℃≦T_A≦85℃	-	±100		ppm/℃

NOTE:
(*1) Unless otherwise stated, V_{IN} = $V_{OUT(T)}$ + 1.0V
(*2) $V_{OUT(E)}$:Effective output voltage.
(*3) $V_{OUT(T)}$:Nominal voltage
(*4) Vdif =V_{IN1} -V_{OUT1}
V_{OUT1}: A voltage equal to 98% of the output voltage whenever an amply stabilized {VOUT(T) + 1.0V} is input with each IOUT.
V_{IN1}: The input voltage when VOUT1 appears as input voltage is gradually decreased.
(*5) Reference value

Functional Block Diagram

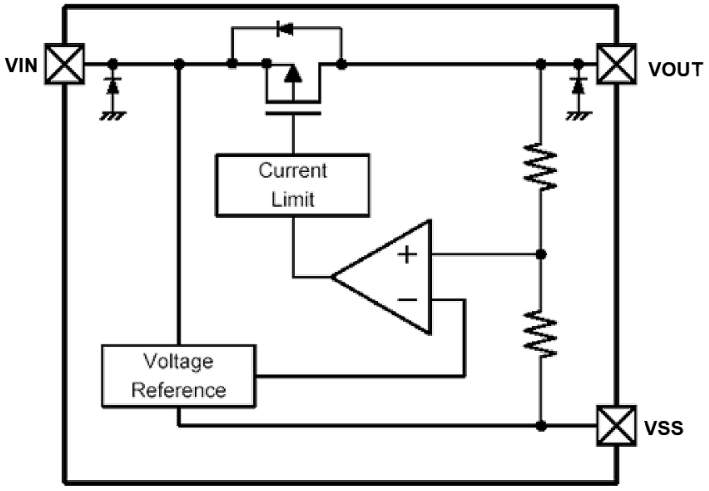

Figure.1 Typical Application Circuit

*Diodes inside the circuit are an ESD protection diode and a parasitic diode.

PRODUCT CLASSIFICATION

- Ordering Information
  LPL1206P①②③④⑤

DESIGNATOR	CONTENTS	SYMBOL	DESCRIPTIONS
①②	V_{OUT}	12～50	e.g. Vout:3.3v→33; 2.0v→20
③	Accuracy	2	2%
④⑤	Package（MOQ）	M3	SOT23-3(3,000pcs/Reel)

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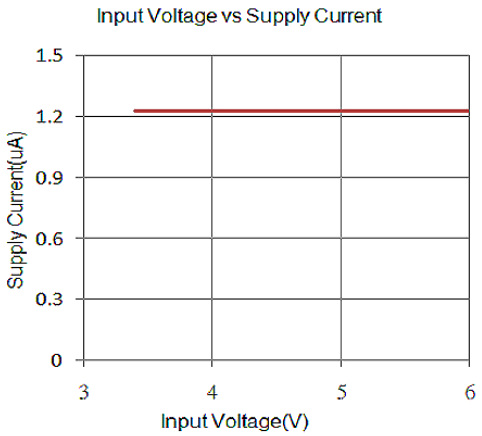
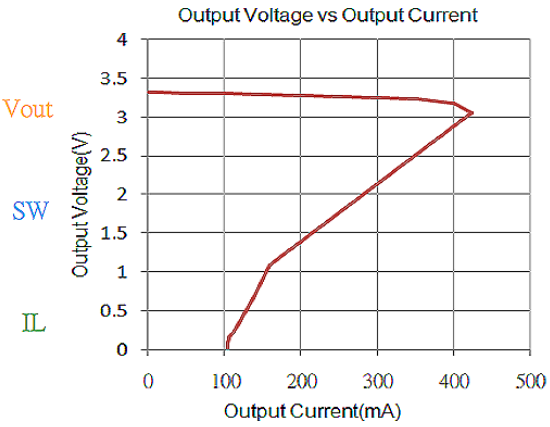
Typical Operating Characteristics

CIN = 1uF, CL = 1uF, TA = +25℃, unless otherwise noted.

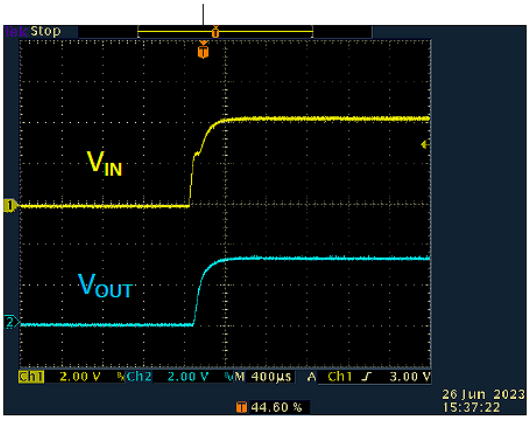
IQ



Current Fold Back

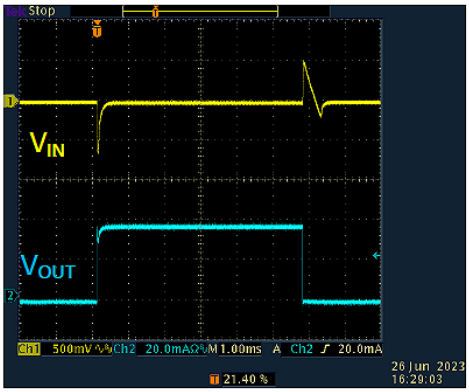


Start-up



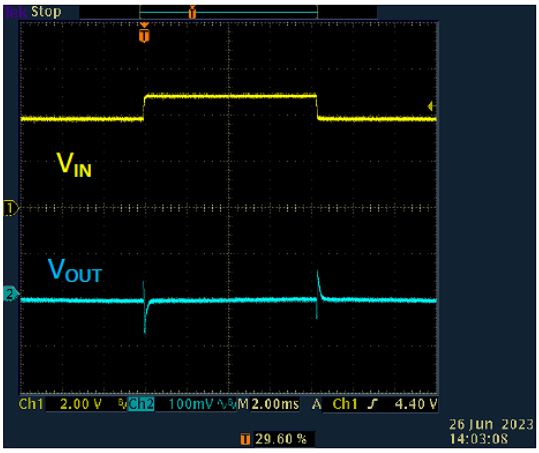
Dynamic loading

Vin=4.3V,Iout=1 to 40mA



Input Transient Response

Iout=10mA



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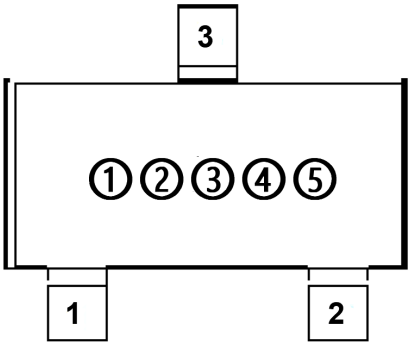
NOTES ON USE:

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please strengthen VIN and VSS wiring in particular.
3. Please wire the input capacitor (CIN) and the output capacitor (CL) as close to the IC as possible.
4. Capacitances of these capacitors (CIN, CL) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.
5. When it is used in a quite small input / output dropout voltage, output may go into unstable operation. Please test it thoroughly before using it in production.
6. **LFC** places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using **LFC** products in their systems.

MARKING RULE

SOT23-3



Ording information	1	2 3		4	5
product number	Product Series: LPL1206P	12	1.2V	production lot number	
		15	1.5V		
		18	1.8V		
		25	2.5		
		28	2.8		
		30	3.0		
		33	3.3		
		36	3.6		
		50	5.0		
		XX	X.X		

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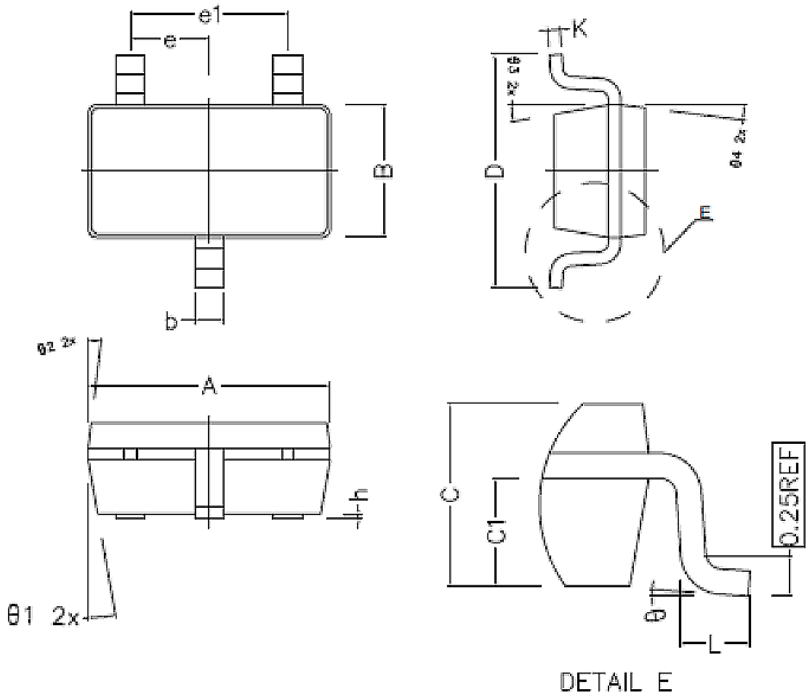
Package Information

SOT-23



UNIT:MM

SYMBOLS	Min	Typ	Max
A	2.820	2.920	3.020
B	1.500	1.600	1.700
C	1.050	1.100	1.150
C1	0.600	0.650	0.700
D	2.650	2.800	2.950
L	0.300	0.450	0.600
b	0.280	0.350	0.420
h	0.020	0.050	0.100
K	0.120	-----	0.230
e	0.950 TYP		
e1	1.900 TYP		
θ1	10°TYP		
θ2	7° TYP		
θ3	10° TYP		
θ4	7° TYP		
θ	0°~8°		

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