

LMN6184DF 60V N-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)}=92m\Omega@V_{GS}=10V$
- $R_{DS(ON)}=100m\Omega@V_{GS}=4.5V$
- Improved dv/dt capability
- Fast switching
- 100% EAS guaranteed.

been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

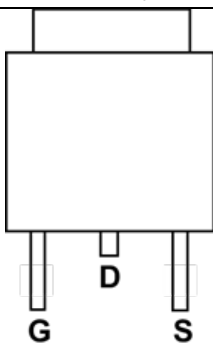
Product Description

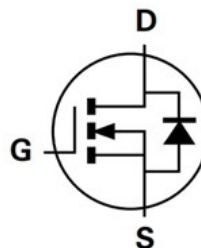
These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has

Applications

- Motor Drive
- Power Tools
- LED Lighting

Pin Configuration

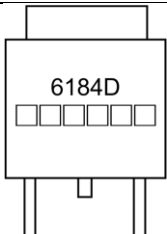
LMN6184DF (TO-252)	
	
Transparent top view	
Pin	Description
1	Gate
2	Drain
3	Source



Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMN6184DF	LMN4184	D	F	TO-252	2500 PCS

Marking Information

Part Marking	Part Number
	6184D

Absolute Maximum Ratings

(T_C=25°C Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V _{DSS}	Drain-Source Voltage	60	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Continuous Drain Current ¹	T _C =25°C	10
		T _C =100°C	6
		T _A =25°C	3
		T _A =70°C	2
I _{DM}	Pulsed Drain Current ²	20	A
I _{AS}	Single Pulse Avalanche Current	11.2	A
E _{AS}	Single Pulse Avalanche Energy ³	6.3	mJ
P _D	Total Power Dissipation ⁴	T _C =25°C	20.8
		T _C =100°C	8.3
		T _A =25°C	2
		T _A =70°C	1.2
T _J	Operating Junction Temperature	-55 to +150	°C
T _{STG}	Storage Temperature Range	-55 to +150	°C
R _{θJC}	Thermal Resistance, Junction to Case ¹	6	°C /W
R _{θJA}	Thermal Resistance-Junction to Ambient ¹	62	°C /W

Electrical Characteristics

(T_C=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	uA
R _{DS(on)}	Drain-Source On-Resistance ²	V _{GS} =10V, I _D =6A		85	92	mΩ
		V _{GS} =4.5V, I _D =3A		90	100	
g _{FS}	Forward Transconductance	V _{DS} =10V, I _D =3A		3.6		S
Dynamic						
Q _g	Total Gate Charge	V _{DS} =48V, V _{GS} =4.5V, I _D =10A		4.9		nC
Q _{gs}	Gate-Source Charge			1.8		
Q _{gd}	Gate-Drain Charge			2.2		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		511		pF
C _{oss}	Output Capacitance			38		
C _{rss}	Reverse Transfer Capacitance			25		
t _{d(on)}	Turn-On Time ^{2,3}	V _{DD} =30V, I _D =3A, V _{GS} =4.5V, R _G =3.3Ω		6		ns
t _r				9		
t _{d(off)}	Turn-Off Time ^{2,3}			18		
t _f				5		
Diode characteristics						
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =10A			1.4	V
I _S	Continuous Source Current ¹	V _G =V _D =0V, Force Current			10	A
t _{rr}	Reverse Recovery Time	I _S =3A, V _{GS} =0V dI/dt=100A/μs		19		nS
Q _{rr}	Reverse Recovery Charge			28		nC

Note:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
3. The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=11.2A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

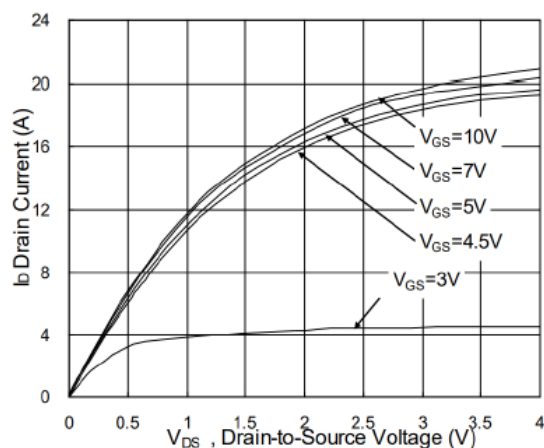


Fig. 1. Output Characteristics

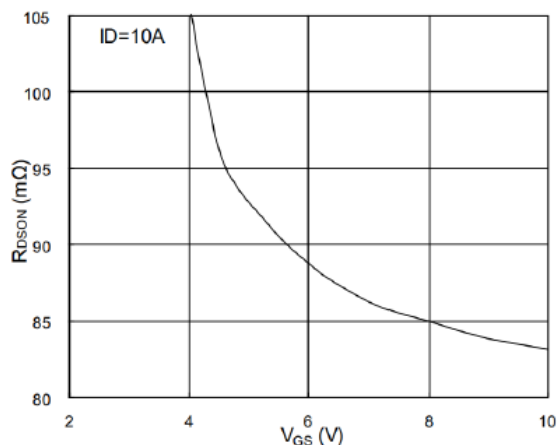


Fig. 2 On-Resistance vs. Gate Source

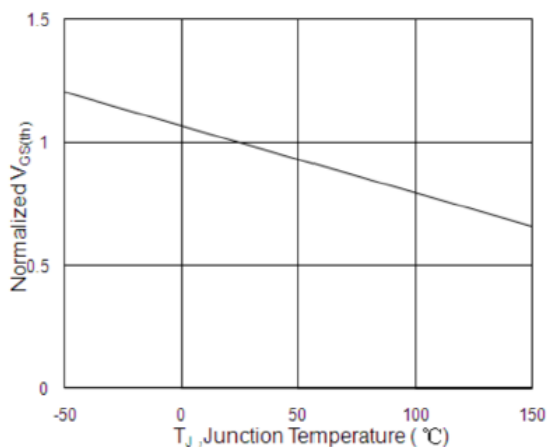


Fig. 3 Normalized Gate Threshold Voltage

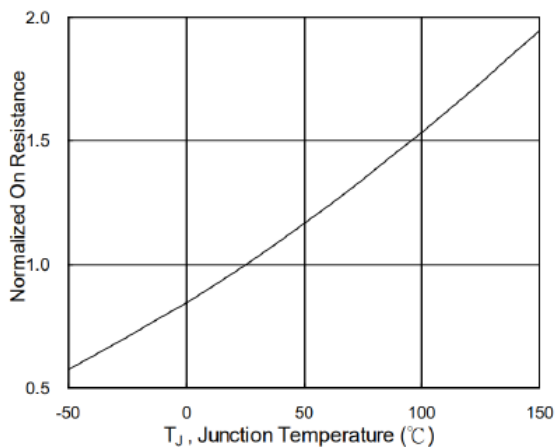


Fig. 4 Normalized On-Resistance

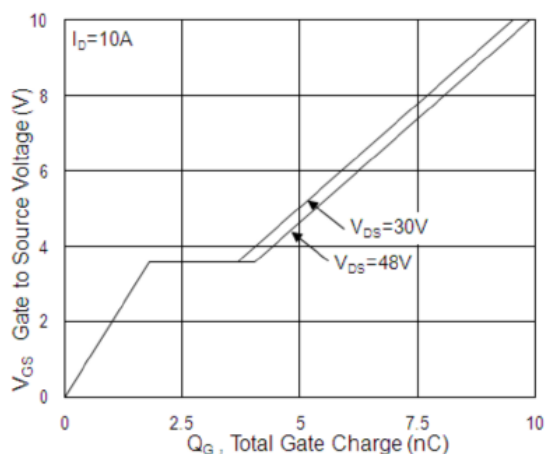


Fig. 5 Gate Charge Characteristics

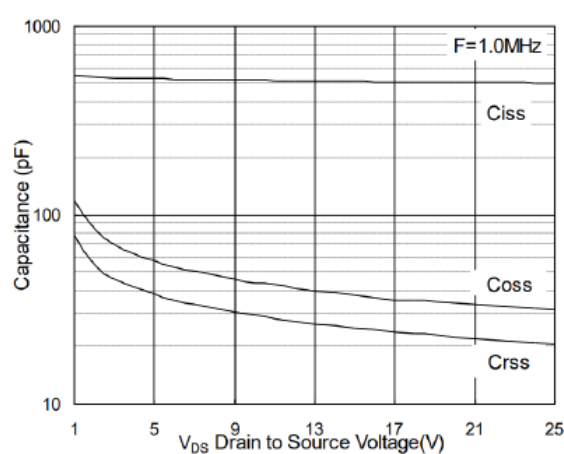


Fig. 6 Typical Capacitance

Typical Performance Characteristics

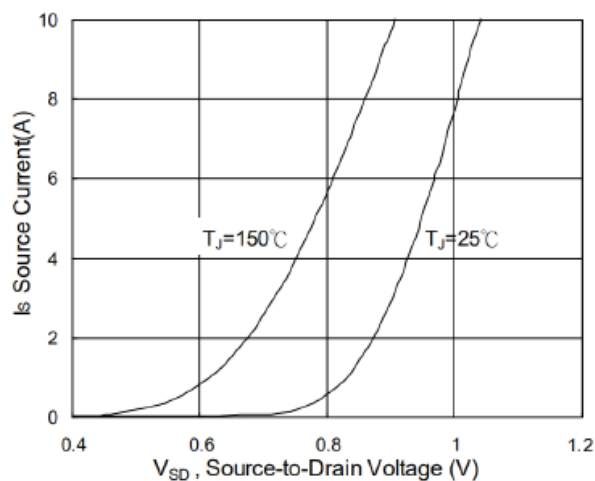


Fig. 7 Diode Forward Characteristics

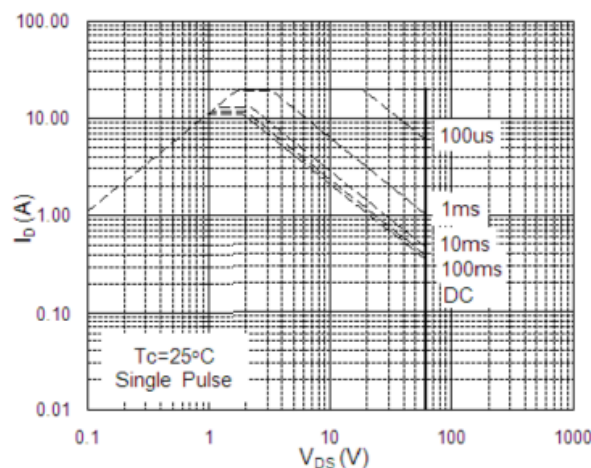


Fig. 8 Safe Operating Area

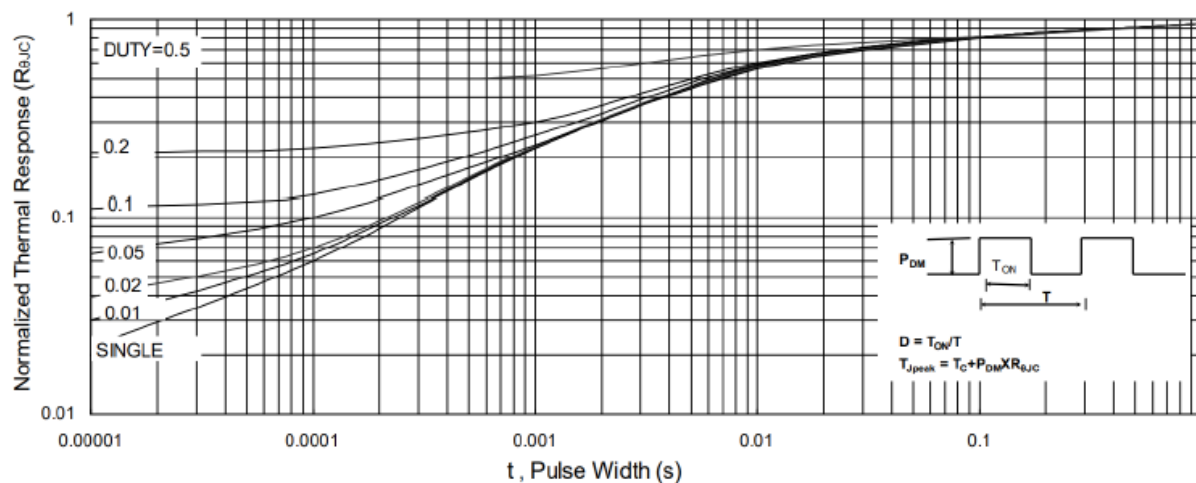
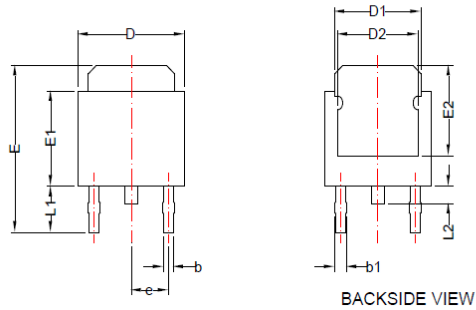


Fig. 9 Transient Thermal Impedance

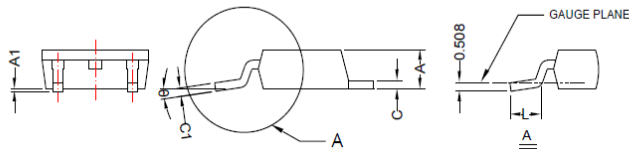
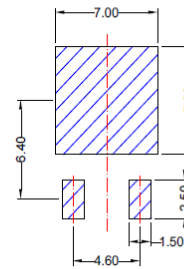
Package Dimension:

TO-252

Package Dimension



Recommended Land Pattern



Symbol	Dimensions			
	Millimeters		Inches	
	Min	Max	Min	Max
A	2.18	2.40	0.086	0.094
A1	0.00	0.15	0.000	0.006
b	0.50	0.90	0.020	0.035
c	0.45	0.89	0.018	0.035
c1	0.40	0.61	0.016	0.024
D	6.35	6.80	0.250	0.268
D1	4.95	5.50	0.195	0.217
D2	3.81	-	0.150	-
E	9.40	10.41	0.370	0.410
E1	5.33	5.80	0.210	0.228
E2	4.57	-	0.180	-
e	2.286 BSC		0.090 BSC	
L	1.40	1.78	0.055	0.070
L1	2.40	3.00	0.094	0.118
θ	0°	8°	0°	8°

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