

## KMN1072KX5F 20V N-Channel Enhancement Mode MOSFET

### Features

- 20V, 1A,  $R_{DS(ON)}=450m\Omega@V_{GS}=4.5V$
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation
- ESD Protected
- SOT-323 package design

### Product Description

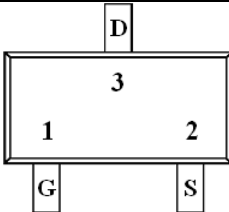
LMN1072 KX5F, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent  $R_{DS(ON)}$ , low

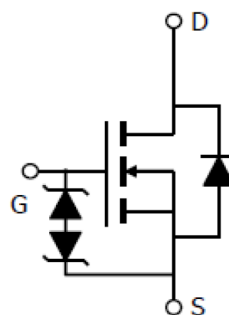
gate charge. These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

### Applications

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Smart Phones, Pagers

### Pin Configuration

LMN1072 KX5F (SOT-323)	
	
PIN	Description
1	Gate
2	Source
3	Drain



## Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMN1072KX5F	LMN1072K	X5	F	SOT-323	3000 PCS

## Marking Information

Marking Information		
Part Marking	Part Number	LFC code
2XWMM	2	XWMM

## Absolute Maximum Ratings

(T<sub>C</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V <sub>DSS</sub>	Drain-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	±10	V
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> =25°C	A
		T <sub>A</sub> =70°C	
I <sub>DM</sub>	Pulsed Drain Current	4	A
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> =25°C	W
		T <sub>A</sub> =70°C	
T <sub>J</sub>	Operating Junction Temperature	-55 to +150	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C
R <sub>θJA</sub>	Thermal Resistance-Junction to Ambient	425	°C/W

**Electrical Characteristics**

(T<sub>C</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	20			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , ID=250uA	0.3		1	
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±10V			±10	uA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V			1	uA
		V <sub>DS</sub> =16V, V <sub>GS</sub> =0V T <sub>J</sub> =85°C			30	
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =4.5V, ID=0.5A		220	450	mΩ
		V <sub>GS</sub> =2.5V, ID=0.4A		280	600	
		V <sub>GS</sub> =1.8V, ID=0.2A		390	750	
		V <sub>GS</sub> =1.5V, ID=0.1A		540	1200	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =0.15A, V <sub>GS</sub> =0V			1.3	V
Dynamic						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =10V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.25A		0.73		nC
Q <sub>gs</sub>	Gate-Source Charge			0.93		
Q <sub>gd</sub>	Gate-Drain Charge			0.12		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V, f=1MHz		60.7		pF
C <sub>oss</sub>	Output Capacitance			9.7		
C <sub>rss</sub>	Reverse Transfer Capacitance			5.4		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =10V, R <sub>L</sub> =47Ω, I <sub>D</sub> =0.2A, V <sub>GS</sub> =4.5V, R <sub>G</sub> =10Ω		5.1		ns
t <sub>r</sub>				7.4		
t <sub>d(off)</sub>	Turn-Off Time			26.7		
t <sub>f</sub>				12.3		

## Typical Performance Characteristics

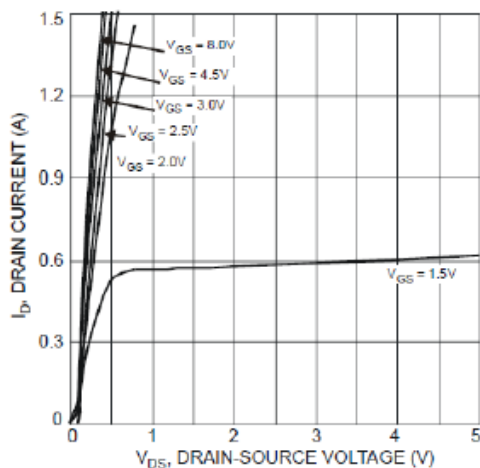


Fig. 1 Typical Output Characteristics

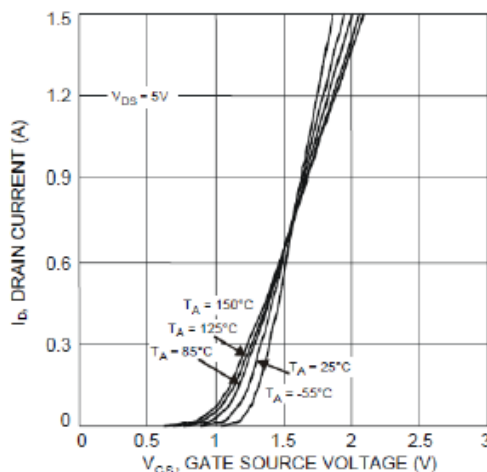


Fig. 2 Typical Transfer Characteristics

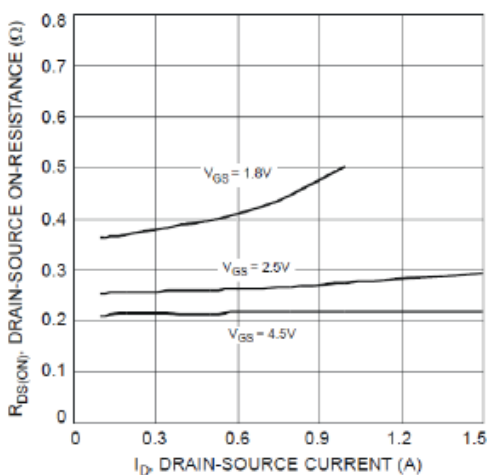


Fig. 3 Typical On-Resistance vs.  $I_D$  and  $V_{GS}$

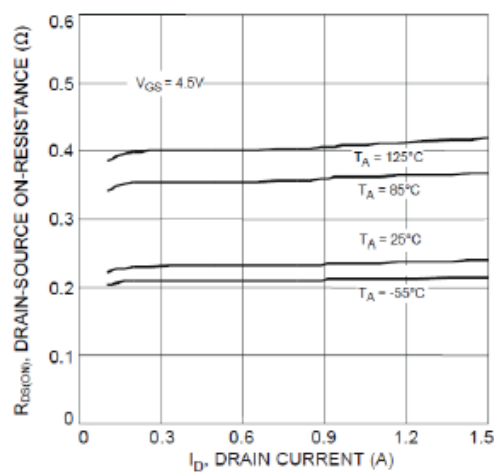


Fig. 4 Typical Drain-Source On-Resistance vs.  $I_D$  and  $T_J$

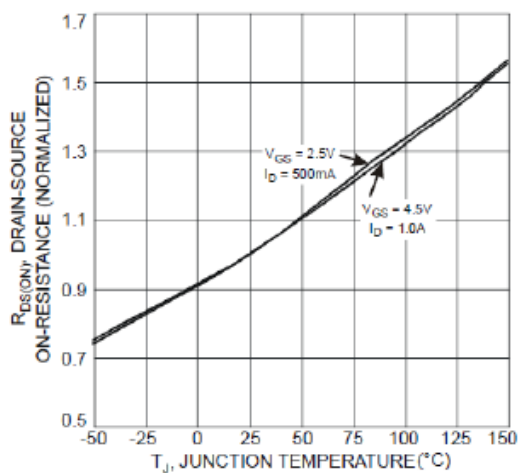


Fig. 5 On-Resistance Variation with  $T_J$

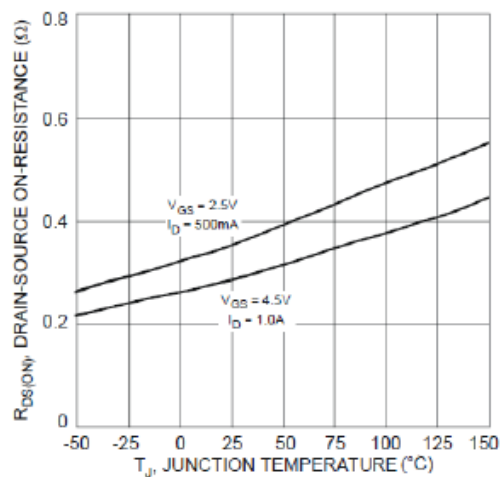
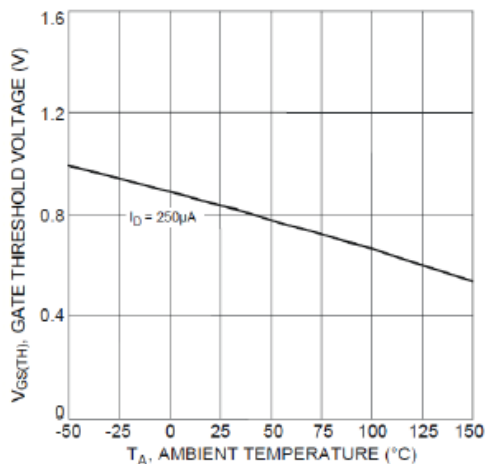
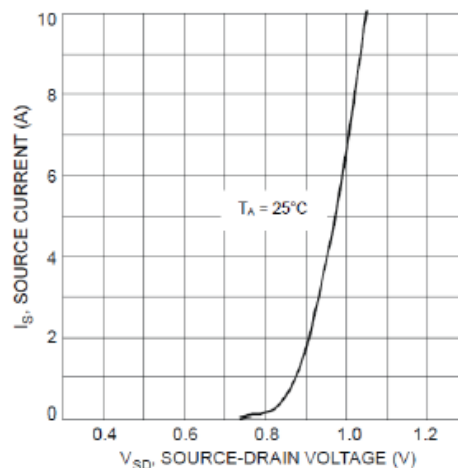
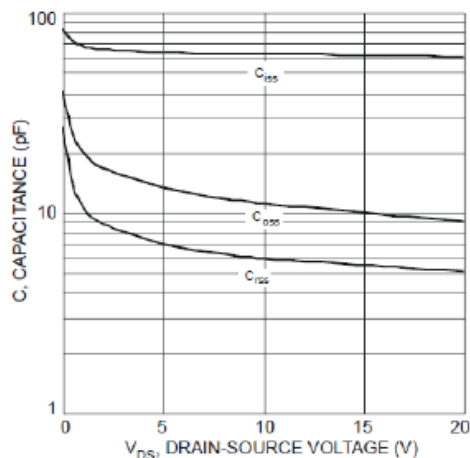
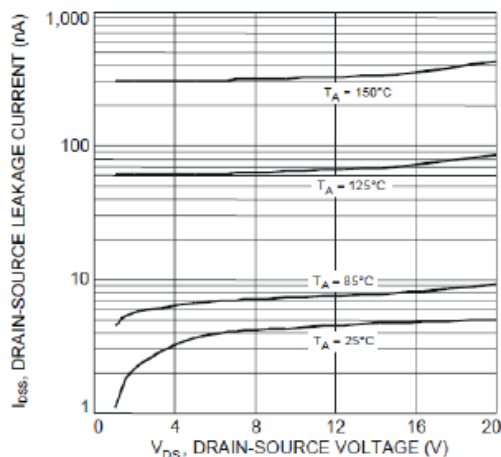
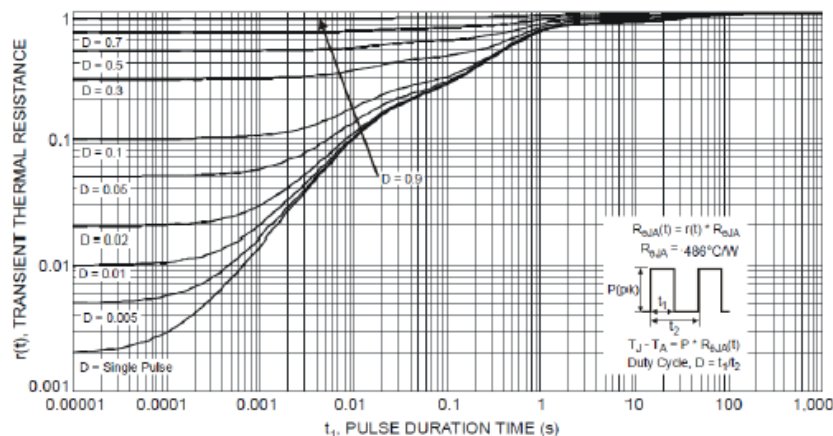


Fig. 6 On-Resistance Variation with  $T_J$

**Typical Performance Characteristics(continue)**

**Fig. 7 Gate Threshold Variation vs.  $T_A$** 

**Fig. 8 Diode Forward Voltage vs. Current**

**Fig. 9 Typical Capacitance**

**Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage**

**Fig. 11 Transient Thermal Response**

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