

LMP02P15TSF 150V P-Channel MOSFET

Features

- -150V/-1A, $R_{DS(ON)}$ <750m Ω @ V_{GS} =-10V
- Fast switching
- Improved dv/dt capability
- Green Device Available
- TSOP-6 package design

Product Description

These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been

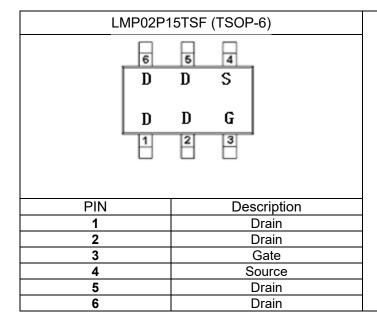
especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

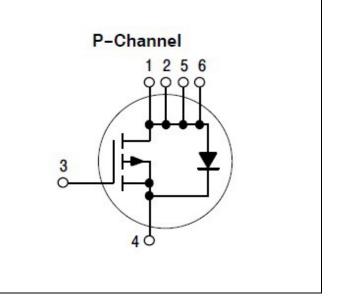
These devices are well suited for high efficiency fast switching applications.

Applications

- Networking
- Load Switch
- LED Application

Pin Configuration







Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP02P15TSF	LMP02P15	TS	F	TSOP-6	3000

Marking Information

Marking Information				
Part Marking	Part Number	LFC code		
25PXW	25P	XW		

Absolute Maximum Ratings

(T_C=25°C Unless otherwise noted)

Symbol	Parameter	Typical	Unit	
V _{DS}	Drain-Source Voltage	-150	V	
V_{GS}	Gate-Source Voltage	±20	V	
I _D	Drain Current- Continuous (Tc=25°C)	-1	Α	
10	Drain Current- Continuous (Tc=100°C)	-0.63	Α	
I _{DM}	Drain Current- Pulsed1	-4	Α	
_	Power Dissipation (Tc=25°C)	1.56	W	
P _D	Power Dissipation –Derate above 25°C	0.012	W/°C	
TJ	Operating Junction Temperature Range	-50 to 150	°C	
Tstg	Storage Temperature Range	-50 to 150	°C	
RθJA	Thermal Resistance-Junction to ambient	80	°C/W	

LMP02P15TSF 2



Electrical Characteristics

(T_C=25°C Unless otherwise noted)

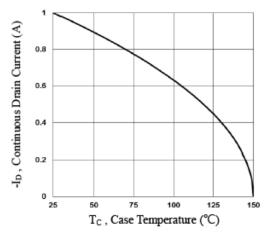
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	•	Static				
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V _{GS} =0V,I _D =250uA	- 150			V
$V_{GS(th)}$	Gate Threshold Voltage	V _{GS} =V _{DS} ,I _D =-250uA	-2	3	-4	
I _{GSS}	Gate-Source Leakage Current	V _{DS} =0V,V _{GS} =±20V			±100	nA
lpss	Drain-Source Leakage Current	V _{DS} =-150V, V _{GS} =0V, T _J =25°C			-1	μΑ
1000		V _{DS} =-120V,V _{GS} =0V,T _J =125°C			-10	
R _{DS(on)}	Drain-Source On-	V _{GS} =-10V,I _D =-1A		650	800	mΩ
1 (D3(011)	Resistance	V _{GS} =-6V,I _D =-0.5A		700	950	
V_{SD}	Diode Forward Voltage	I _S =-1A,V _{GS} =0V, T _J =25°C			-1	V
Is	Continuous Source Current	V _{GS} =V _D =0V,Force Current			-1	А
I _{SM}	Pulsed Source Current				-2	Α
g FS	Forward Transconductance	V _{DS} =-10V,I _D =1A		2		S
Rg	Gate resistance	V _{DS} =0V, V _{GS} =0V, F=1MHz		30	60	Ω
		Dynamic				
Ciss	Input Capacitance			430	700	
C_{oss}	Output Capacitance	V _{DS} =-25V, V _{GS} =0V, F=1MHz		38	60	pF
Crss	Reverse Transfer Capacitance			28	56	
Q_g	Total Gate Charge ^{2,3}			4.4	8	
Q_gs	Gate-Source Charge ^{2,3}	V _{DS} =-75V, V _{GS} =10V, I _D =-1A		0.7	2	nC
Q_{gd}	Gate-Drain Charge ^{2,3}			1.5	3	
$t_{d(on)}$	Turn-On Time ^{2,3}			12.5	20	8 ns
tr		- V _{DD} =-75V, V _{GS} =-10V, R _G =10Ω, I _D =-1A		8.9	18	
$t_{d(off)}$	Turn-Off Time ^{2,3}			17.3	36	
t _f				11.5	24	

Note:

- 1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
- 2. The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%.
- 3. Essentially independent of operating temperature.



Typical Performance Characteristics



Continuous Drain Current vs. Tc

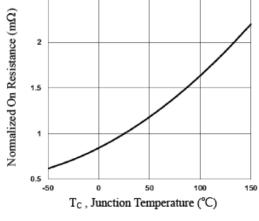
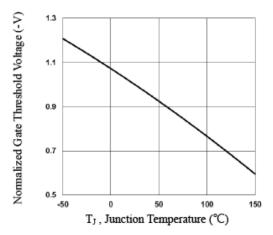
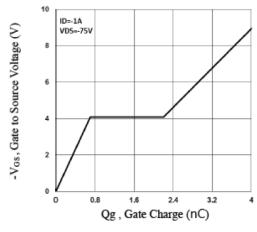


Fig.2 Continuous Drain Current vs. Tc



Normalized Vth vs. TJ



Gate Charge Waveform

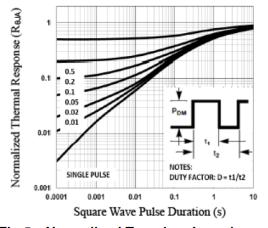


Fig.5 Normalized Transient Impedance

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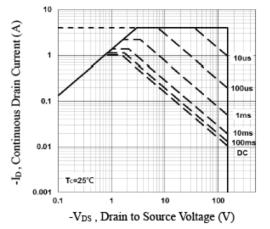


Fig.6 Maximum Safe Operation Area



Typical Performance Characteristics(continue)

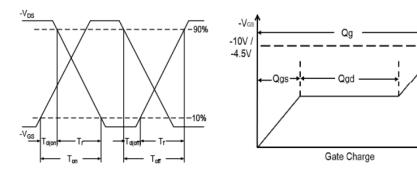
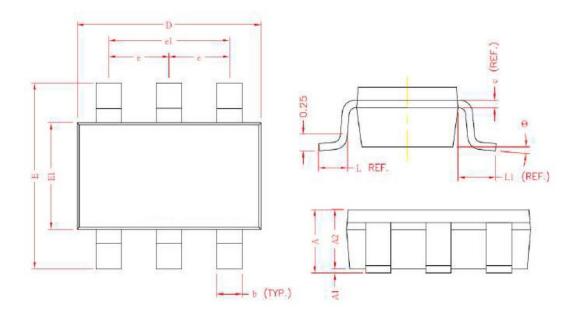


Fig.7 Switching Time Waveform

Fig.8 Gate Charge Waveform

Package Dimension:

TSOP-6



LMP02P15TSF 5



		Dimensions	3		
	Millim	eters	Inc	hes	
Symbol	Min	Max	Min	Max	
Α	-	1.45	-	0.057	
A1	0.00	0.10	0.000	0.004	
A2	0.70	1.35	0.028	0.053	
С	0.12 (REF)		0.005 (REF)		
D	2.70	3.10	0.106	0.122	
E	2.60	3.00	0.102	0.118	
E1	1.40	1.80	0.055	0.071	
L	0.45 (REF)		0.018 (REF)		
L1	0.60 (REF)		0.024 (REF)		
θ	0 °	10 °	0 °	10 °	
b	0.30	0.50	0.012	0.020	
е	0.95 (REF)		0.037 (REF)		
e1	1.90 (RE	<u>.</u> :F)	0.075 (R	EF)	

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