

## LMP3825EX5F 30V P-Channel MOSFET

### Features

- -30V/-0.5A,  $R_{DS(ON)} < 2500m\Omega @ V_{GS} = -4.5V$
- -30V/-0.2A,  $R_{DS(ON)} < 2900m\Omega @ V_{GS} = -2.5V$
- -30V/-0.1A,  $R_{DS(ON)} < 5000m\Omega @ V_{GS} = -1.8V$
- Low-Voltage Operation
- High-Speed Circuits
- ESD Protection
- SOT-323 package design

### Product Description

LMP3825EX5F, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide

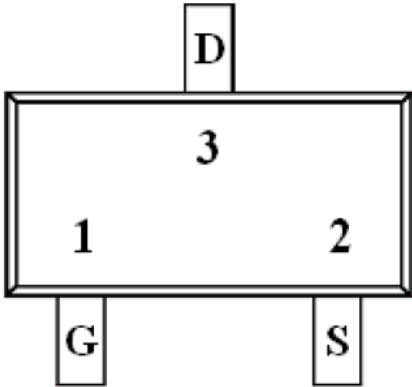
excellent  $R_{DS(ON)}$ , low gate charge.

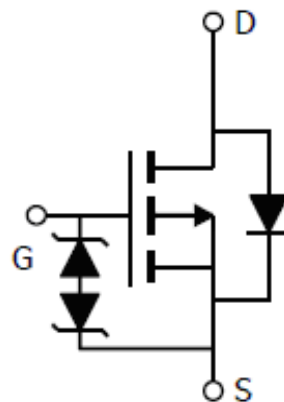
These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

### Applications

- Drivers, Relays, Solenoids, Lamps, Hammers
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Smart Phones, Pagers

### Pin Configuration

LMP3825EX5F (SOT-323)	
	
PIN	Description
1	Gate
2	Source
3	Drain



**Ordering Information**

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3825EX5F	LMP3825E	X5	F	SOT-323	3000

**Marking Information**

Marking Information		
Part Marking	Part Number	LFC code
5XWMM	5	XWMM

**Absolute Maximum Ratings**

(T<sub>C</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Typical	Unit
V <sub>DSS</sub>	Drain-Source Voltage	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	±10	V
I <sub>D</sub>	Continuous Drain Current (T <sub>J</sub> =150°C)	T <sub>A</sub> =25°C	A
		T <sub>A</sub> =70°C	
I <sub>DM</sub>	Pulsed Drain Current	-1.4	A
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> =25°C	W
		T <sub>A</sub> =70°C	
R <sub>θJA</sub>	Thermal Resistance Junction to ambient	250	°C/W
T <sub>J</sub>	Operating Junction Temperature Range	-55 to +150	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to +150	°C

Note1. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

**Electrical Characteristics**

(T<sub>C</sub>=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
Static						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-0.4		-1.0	
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V			±10	uA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V			-1	uA
R <sub>DS(on)</sub>	Drain-Source On-Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-0.5A		1.5	2.5	Ω
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-0.2A		1.9	2.9	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-0.1A		2.4	5.0	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-0.25A		610		mS
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-0.5A, V <sub>GS</sub> =0V			1.3	V
Dynamic						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A		1.0		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =-15V, V <sub>GS</sub> =-8V, I <sub>D</sub> =-1A		0.2		
Q <sub>gd</sub>	Gate-Drain Charge			0.1		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V f=1MHz		54		pF
C <sub>oss</sub>	Output Capacitance			10.9		
C <sub>rss</sub>	Reverse Transfer Capacitance			5.8		
t <sub>d(on)</sub>	Turn-On Time	V <sub>DD</sub> =-10V, R <sub>L</sub> =47Ω, I <sub>D</sub> ≡-0.2A V <sub>GEN</sub> =-4.5V, R <sub>G</sub> =10Ω		3.8		ns
t <sub>r</sub>				11		
t <sub>d(off)</sub>	Turn-Off Time			45		
t <sub>f</sub>				20		

## Typical Performance Characteristics

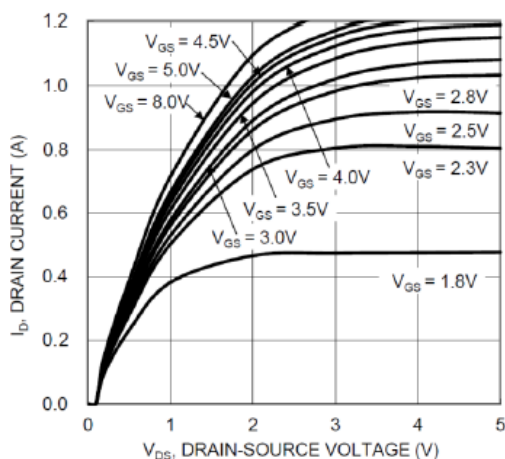


Fig. 1 Typical Output Characteristics

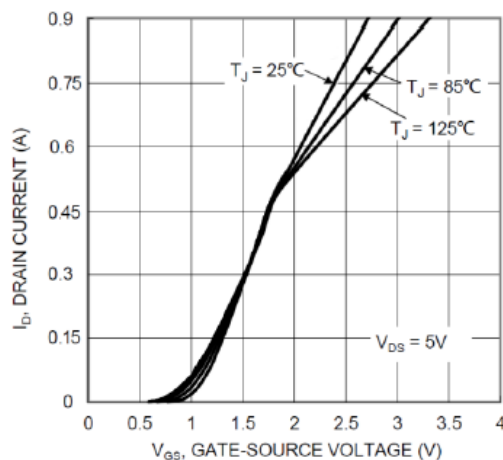


Fig. 2 Typical Transfer Characteristics

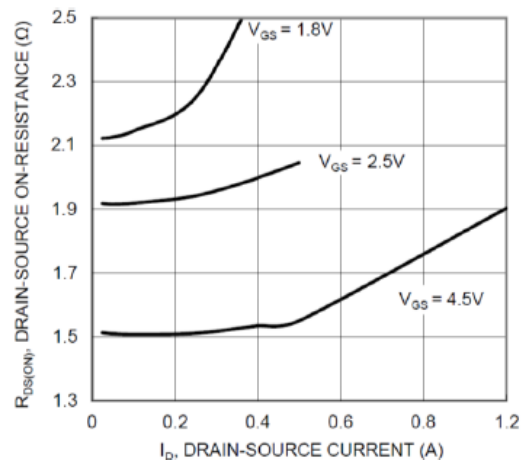


Fig. 3 Typical On-Resistance vs.  $I_D$  and  $V_{GS}$

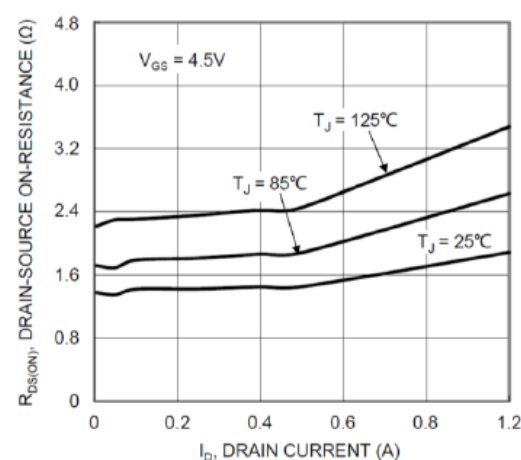


Fig. 4 Typical Drain-Source On-Resistance vs.  $I_D$  and  $T_J$

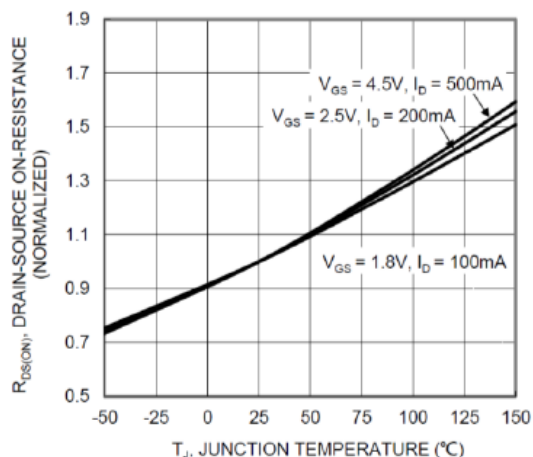


Fig. 5 On-Resistance Variation with  $T_J$

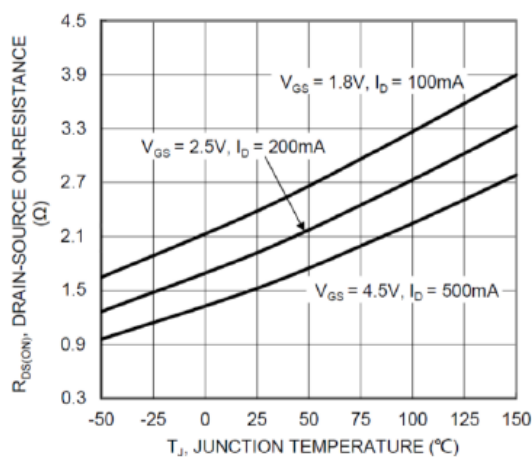


Fig. 6 On-Resistance Variation with  $T_J$

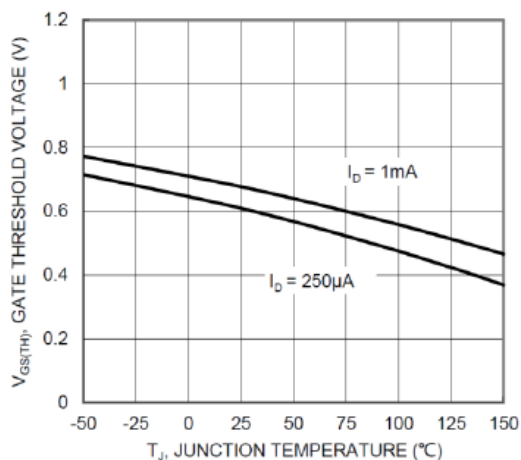
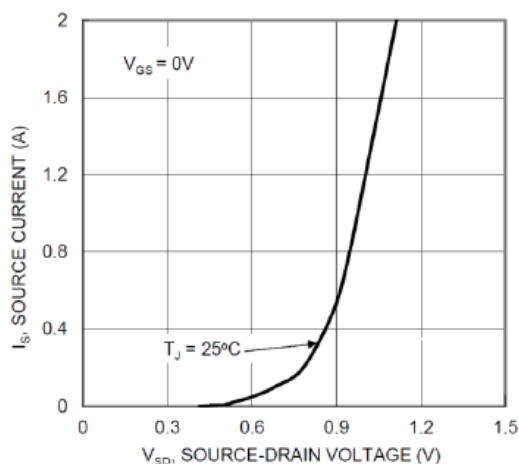
**Typical Performance Characteristics(continue)**

Fig. 7 Gate Threshold Variation vs.  $T_A$ 


Fig. 8 Diode Forward Voltage vs. Current

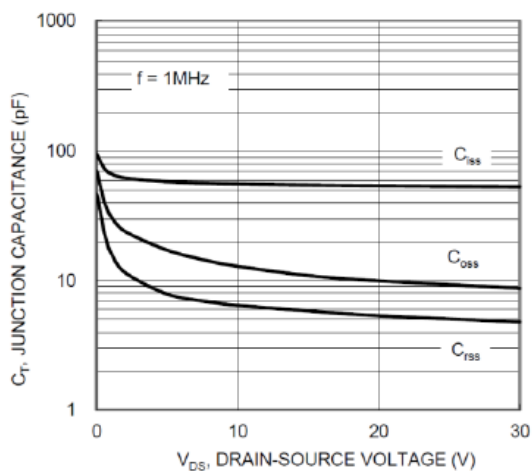


Fig. 9 Typical Capacitance

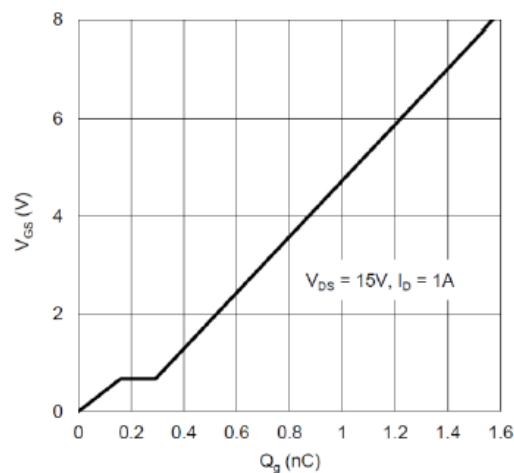


Fig. 10 Gate Charge

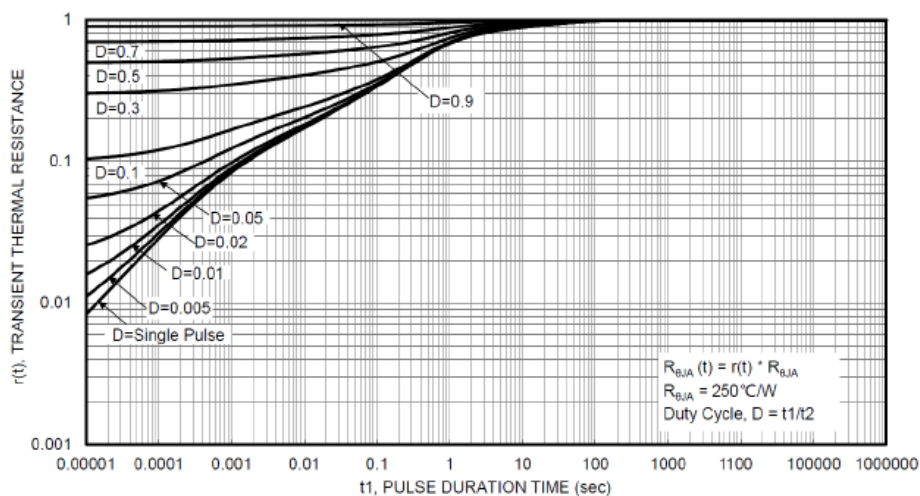
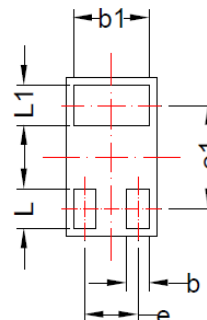
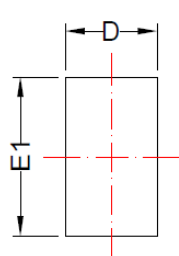
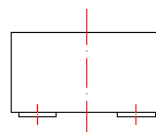
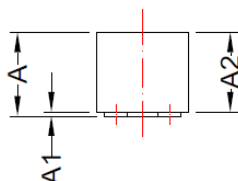


Fig. 11 Transient Thermal Response

**Package Dimension:**
**DFN1006-3L**

**BACKSIDE VIEW**


DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE FOR VARIATIONS WITH BODY SIZES =3x3mm. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 mm FOR VARIATIONS WHERE EITHER D OR E1 IS <3mm.

Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	0.80	1.10	0.031	0.043
<b>A1</b>	0.00	0.10	0.000	0.004
<b>A2</b>	0.80	1.00	0.031	0.039
<b>b</b>	0.20	0.40	0.008	0.016
<b>c</b>	0.08	0.26	0.003	0.010
<b>D</b>	1.80	2.20	0.071	0.087
<b>E</b>	1.80	2.40	0.071	0.094
<b>E1</b>	1.15	1.35	0.045	0.053
<b>e</b>	0.65 BSC		0.026 BSC	
<b>L</b>	0.26	0.45	0.010	0.018
<b>θ</b>	0°	8°	0°	8°

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