LO210 Series

Low Jitter & Low Power Oscillator

Features

- Frequency range 20MHz ~ 40MHz
- Supply voltage 1.62V ~ 3.63V
- CMOS output
- Operating temperature -40~125ºC
- SMD seam sealing ceramic package
- RoHS compliant & Pb free
- 2.5mm x 2.0mm
- AEC-Q100 G1

Electrical Specifications

Item	Specification
Frequency	20MHz ~ 40MHz
Supply Voltage (VDD)	1.8V ~ 3.3V [1], ±10%
Output Type	CMOS
Output Load	15 pF
Oscillation Mode	Fundamental
Frequency Stability	±50 ppm [1] [2]
Operation Temperature Range	-40ºC ~ 125ºC [1]
Storage Temperature Range	-55ºC ~ 125ºC
Output Voltage Low (V_{OL}) @ VDD = 3.3V, I_{OL} = 12mA @ VDD = 1.8V, I_{OL} = 4mA	0.2VDD Max.
Output Voltage High (V_{OH}) @ VDD = 3.3V, I_{OH} = -12mA @ VDD = 1.8V, I_{OH} = -4mA	0.8VDD Min.
Rise(Tr) / Fall(Tf) Time [3]	6 ns Max.
Dynamic Supply Current [4]	2.5mA
Duty Cycle [5]	45% ~ 55%
Start-Up Time	1 ms Max.
Phase Jitter (12kHz~5MHz)	0.5 ps Max. [4]
Aging (at 25ºC)	±3 ppm/year Max.

[1] Ordering options

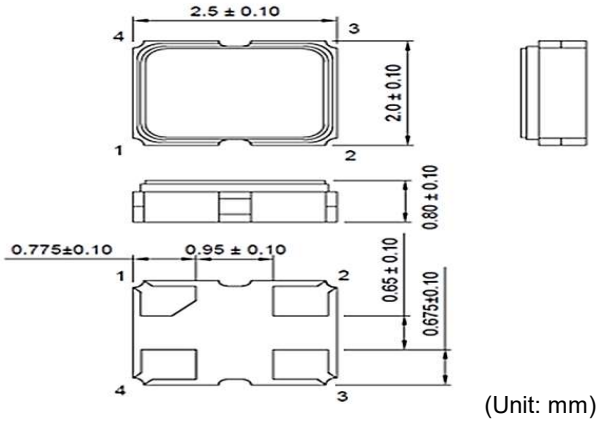
[2] Inclusive of frequency tolerance at 25°C, variations over operating temperature, supply voltage, load and 1st year aging at 25°C.

[3] Tr measure between 10% to 90%, Tf measure between 90% to 10% at 15pF load and V_{DD} 1.8V~3.3V

[4] Measure at 24MHz, V_{DD} 1.8V

[5] Measure at V_{DD} /2

Dimensions

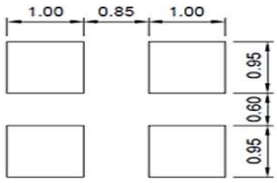


(Unit: mm)

Pad Function

1 EN
2 GND
3 OUTPUT
4 VDD

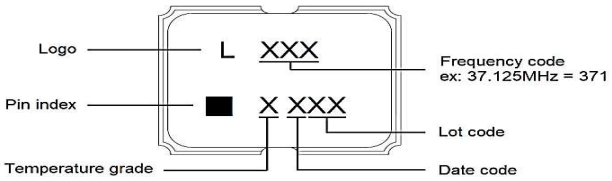
Suggested Layout



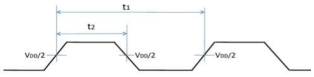
Pin Definition

Pin#	Symbol	Functionality
1	EN	Output Clock Mode Enable Pin H (Logic "1") : Enable L (Logic "0") : High-Z Internal pull-high resistor
2	GND	System ground reference
3	OUTPUT	Oscillator output
4	VDD	System power supply

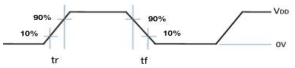
Marking



Duty Cycle Timing

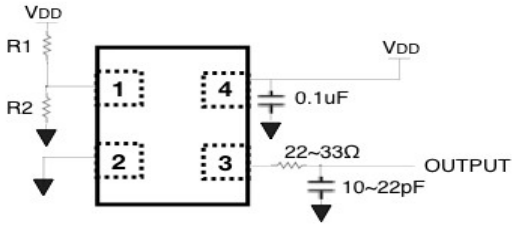


Output Rise/Fall Timing



Temperature grade	Temperature range	Frequency stability (ppm)
A	-40ºC ~ 125ºC	±50

Schematics



Ordering Information

LO210 A - 24M - 50 - C

Product series

Operating temperature range
A : -40~125°C

Frequency in Hz

Frequency stability
50: +/-50ppm

Supply voltage
A : 3.3V
C : 1.8V