

**EMI Reduction Oscillator**
**Features**

- FCC approved method of EMI attenuation
- Proprietary SaΦic™ technology, a non-PLL phase modulation implementation and algorithm Supply
- Voltage 1.65V~1.95V
- Frequency range 20~30Mhz
- CMOS Output
- Modulated clock output Enable/Disable Function
- Low EMI buffer for enhanced EMI reduction
- RoHS compliant & Pb free
- Products available in AEC-Q100 compliant
- Package 2.5x2.0mm,2.0x1.6mm

**Applications**

- SATA, Ethernet, PCI express, Video, Wireless
- Computing, Storage, Networking, Telecom, Industrial Control

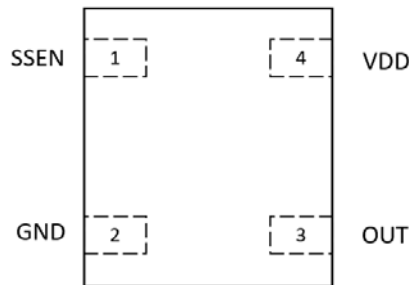
**Table1. Electrical Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Condition
Output Frequency Range	F	20	-	30	MHz	V <sub>DD</sub> =1.8V
Frequency Stability	F <sub>stab</sub>	-30		+30	PPM	Inclusive of initial tolerance at 25 °C, and variations over operating temperature, rated power supply voltage and load.
		-50		+50		
		-60		+60		
		-100		+100		
Operating Temperature Range	T <sub>USE</sub>	-40		+125	°C	
Supply Volage	V <sub>DD</sub>	1.65	1.8	1.95	V	
Output Load	C <sub>L</sub>			9	pF	
Current Consumption	I <sub>DD</sub>	-	4.0	5.0	mA	9pF Load, f=27MHz, V <sub>DD</sub> =1.8V
SSEN mode current	I <sub>SS</sub>		3.0	3.5	mA	When SSEN=GND, 9pF Load, f=27MHz, V <sub>DD</sub> =1.8V output is Pulled Down
Duty Cycle	DC	45		55	%	
Rise/Fall Time	T <sub>r</sub>	5.5	6.0	7.0	nS	9pF load, 10%~90% V <sub>DD</sub> , high drive (V <sub>DD</sub> =1.8V)
	T <sub>f</sub>	6.0	6.5	7.5	nS	
Output Voltage High	V <sub>OH</sub>	0.75* V <sub>DD</sub>	-	-	V	I <sub>OH</sub> =-4mA, I <sub>OL</sub> =4mA
Output Voltage Low	V <sub>OL</sub>	-	-	0.25* V <sub>DD</sub>	V	
Input Voltage High	V <sub>IH</sub>	0.66* V <sub>DD</sub>	-	-	V	
Input Volage Low	V <sub>IL</sub>	-	-	0.33* V <sub>DD</sub>	V	
Startup Time	T <sub>start</sub>	-		1	mS	Measure from the time V <sub>DD</sub> reaches its rated minimum value.
RMS Phase Jitter	T <sub>phj</sub>	-	0.63		pS	F=27MHz, integration bandwidth=12KHz to 5MHz, SSEN=GND
First year Aging	F <sub>aging</sub>	-1.5		+1.5	PPM	25 °C
10-year Aging		-3		+3	PPM	

**Table2. Pin Configuration**

Pin	Symbol	Functionality	
1	SSEN	Input	Modulation Output Clock Mode Enable Pin H (Logic "1") : Enable L (Logic "0") : Disable Internal pull-high resistor
2	GND	Power	Electrical ground
3	OUT	Output	Phase modulated buffered output
4	VDD	Power	Power supply voltage

**TOP View**



**Table3. Deviation select Table**

Deviation Select	1	2	3	4
Frequency	Deviation			
24MHz	±0.61%	±0.39%	±0.28%	±0.22%
25MHz	±0.66%	±0.41%	±0.30%	±0.23%
27MHz	±0.72%	±0.46%	±0.34%	±0.27%

Notes: 1. Please refer to ordering information for deviation select

**Test Circuit and Waveform**

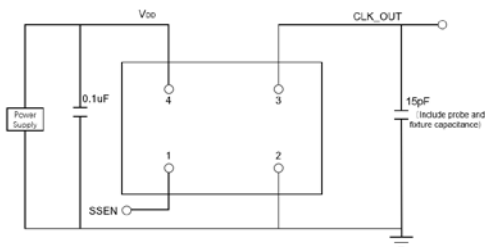


Figure 1. Test Circuit

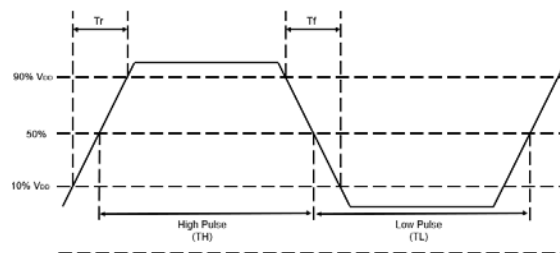
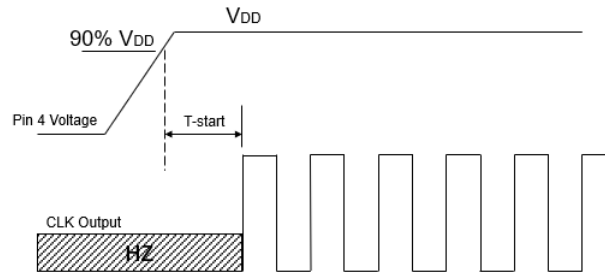


Figure 2. Waveform

Notes: 2. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagram



T-start: Time to start from power-off

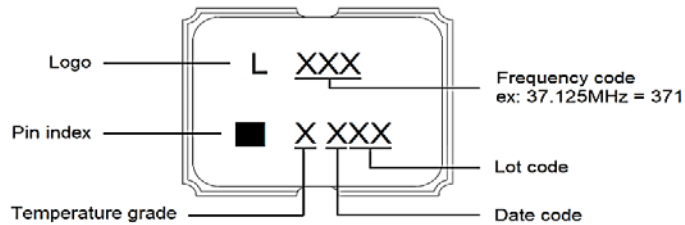
Figure 3. Startup Timing

Ordering Information

**LO6x3 I-24.576M-50-C-1**

<p>Package Size 0: 2016 1: 2520</p>	<p>Frequency in Hz Ex: 24M 27M</p> <p>Frequency stability 30: +/-30PPM; 50: +/-50PPM 60: +/-60PPM; 100: +/-100PPM</p>	<p>Deviation Select Ex: 27MHz 1: ±0.72%; 2: ±0.46% 3: ±0.34%; 4: ±0.27%</p> <p>Supply Voltage C: 1.8V</p>
<p>Operation Temperature I: -40~85°C E: -40~105°C A: -40~125°C</p>		

Marking



Temperature grade	Temperature range	Frequency stability (ppm)
I	-40°C ~85°C	±30
E	-40°C ~ 105°C	±50 / ±60
A	-40°C ~125°C	±50 / ±100

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**Revision History**

Revision Number	Date of Release	Changes
1.0	04/07/2021	1) Preliminary datasheet
1.1	06/01/2021	1) Modify Pin1 function, frequency range, $T_r$ , $T_f$ .
1.2	06/07/2021	1) Modify $I_{DD}$ , $I_{SS}$