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**EMI Reduction Oscillator**


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**Features**

- FCC approved method of EMI attenuation
- Proprietary “SaΦic™” technology
- Supply voltage 1.65V~1.95V
- Frequency range 1~125Mhz
- Output Multiple Deviation Selections
- Minimum frequency deviation selection capability
- Pin1 modes: output enable or spread disable
- Package QFN:3.2x2.5mm

**Applications**

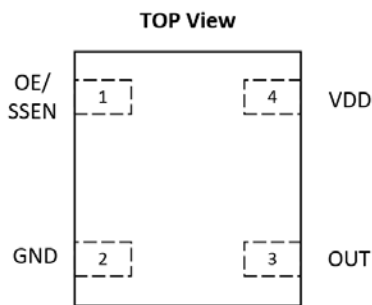
- SATA, Ethernet, PCI express, Video, Wireless
- Computing, Storage, Networking, Telecom, Industrial Control

**Table1. Electrical Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Condition
Output Frequency Range	F	1	-	125	MHz	V <sub>DD</sub> =1.8V
Frequency Stability	F <sub>stab</sub>	-10		+10	PPM	Inclusive of initial tolerance at 25 °C, and variations over operating temperature, rated power supply voltage and load.
		-20		+20		
		-50		+50		
Operating Temperature Range	T <sub>use</sub>	-40		+85	°C	
Supply Voltage	V <sub>DD</sub>	1.65	1.8	1.95	V	
Current Consumption	I <sub>DD</sub>	-		28	mA	No load condition, f=100MHz, V <sub>DD</sub> =1.8V
OE mode disable current	I <sub>od</sub>			18	mA	When OE=GND, output is Pulled Down
Duty Cycle	DC	45		55	%	Please refer figure 2
Rise/Fall Time	T <sub>r</sub> , T <sub>f</sub>		1.5		nS	15pF load, 10%~90% V <sub>DD</sub> , high drive (V <sub>DD</sub> =1.8V)
Output Voltage High	V <sub>OH</sub>	V <sub>DD</sub> -0.4	-	-	V <sub>DD</sub>	I <sub>OH</sub> =-4mA, I <sub>OL</sub> =4mA, Standard Drive
Output Voltage Low	V <sub>OL</sub>	-	-	0.4	V <sub>DD</sub>	
Input Voltage High	V <sub>IH</sub>	70%	-	-	V <sub>DD</sub>	Pin1, OE
Input Voltage Low	V <sub>IL</sub>	-	-	30%	V <sub>DD</sub>	Pin1, OE
Startup Time	T <sub>start</sub>	-	5	7	mS	Measure from the time V <sub>DD</sub> reaches its rated minimum value.
OE Enable/Disable Time	T <sub>oe</sub>	-	-	10	nS	OE function; Ta=25 °C, 15pF load. Add one clock period to this measurement for a usable clock output.
PK-PK Period Jitter	T <sub>jitt</sub>	-	200	350	pS	F=100MHz, V <sub>DD</sub> =1.8V
First year Aging	F <sub>aging</sub>	-1.5		+1.5	PPM	25 °C
10-year Aging		-5		+5	PPM	

**Table2. Pin Configuration**

Pin	Symbol		Functionality
1	OE/ SSEN	Output Enable	H or Open, Specified frequency output L: output is high impedance. Only output driver is disable
		Spread Disable	H: Spread = ON L: Spread = OFF
2	GND	Power	Electrical ground
3	OUT	Output	Oscillator output
4	VDD	Power	Power supply voltage



**Table3. Deviation select Table**

Deviation Select	1	2	3	4
Deviation	±0.69%	±0.44%	±0.32%	±0.25%

Notes: Please refer to ordering information for deviation select.

**Test Circuit and Waveform**

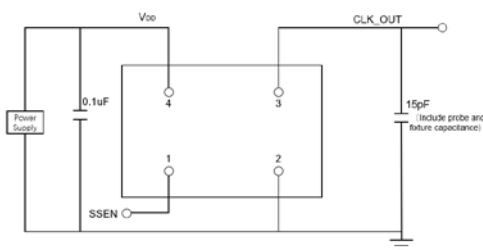


Figure 1. Test Circuit

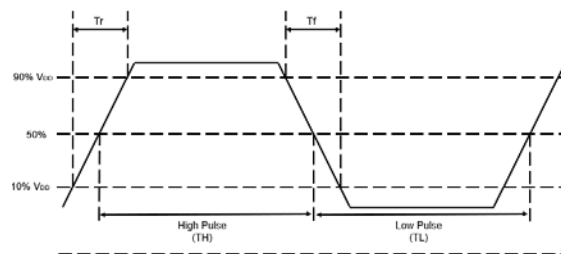
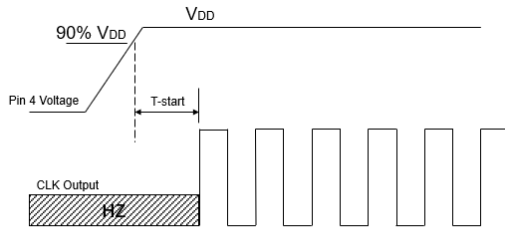


Figure 2. Waveform

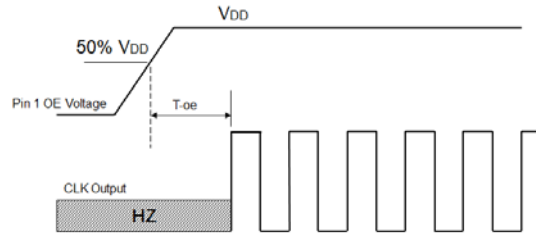
Notes: Duty Cycle is computed as Duty Cycle = TH/Period.

### Timing Diagram



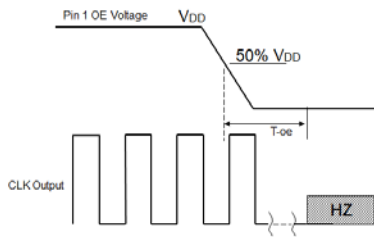
T-start: Time to start from power-off

Figure 3. Startup Timing



T-oe: Time to re-enable the clock output

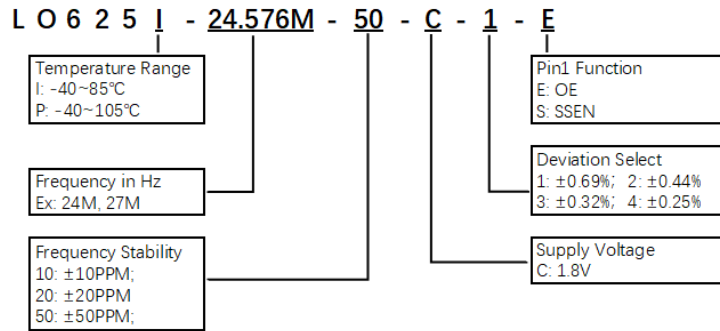
Figure 4. OE Enable Timing



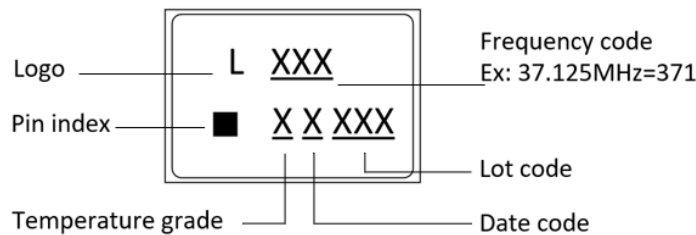
T-oe: Time to re-enable the clock output

Figure 5. OE Disable Timing

### Ordering Information

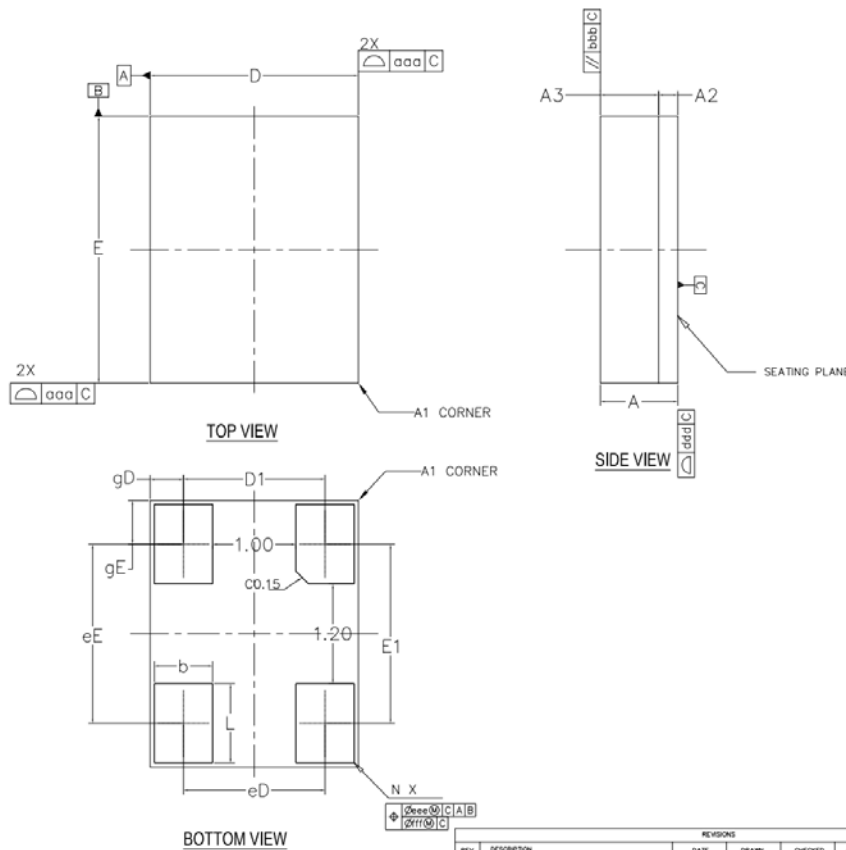


### Marking



Temperature Grade	Temperature Range	Frequency Stability (PPM)
I	-40~85°C	±10 / ±20 / ±50
P	-40~105°C	±10 / ±20 / ±50

## Package Dimension



### COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

Item	Symbol	Common Dimensions			
		MIN.	NOM.	MAX.	
Body Size	X	D	2.400	2.500	2.600
	Y	E	3.100	3.200	3.300
Pin Pitch	X	eD	1.700		
	Y	eE	2.150		
Mold Thickness	A3	0.700 Ref.			
Substrate Thickness	A2	0.200	0.230	0.260	
Total Thickness	A	0.880	0.930	0.980	
Pin	b	0.650	0.700	0.750	
	L	0.900	0.950	1.000	
Package Edge Tolerance	aaa	0.150			
Mold Flatness	bbb	0.100			
Coplanarity	ddd	0.050			
Pin Offset (Package)	eee	0.080			
Pin Offset (Pin)	fff	0.100			
Pin Count	n	4			
Edge Pin Center to Center	X	D1	1.700		
	Y	E1	2.150		
Edge Pin Center to Package Edge	X	gD	0.400		
	Y	gE	0.525		

TONGFU MICROELECTRONICS CO.,LTD

UNLESS OTHERWISE SPECIFIED PROJECTION TITLE: LGA4NT2.5X3.2L-070

## Revision History

Revision Number	Date of Release	Changes
1.0	04/07/2021	1)Preliminary datasheet
1.1	05/06/2021	1)Add temperature grade P
1.2	05/25/2021	1)Update the pin configuration and ordering information, delete the PDB function
1.3	06/18/2021	1)Update package dimension