

1.65V – 3.6V, 1x Ultra Low Power Mobile EMI Reduction IC

**Features**

- FCC approved method of EMI attenuation.
- Generates a 1X low EMI Phase Modulated replication of the input signal.
- Vdd 1.65V -3.6V 1MHz to 10MHz
- Multiple Deviation Selections
- Power save mode
- 8-pin DFN package
- **AEC-Q100 Grade 1 and Grade 2 certified**

**Product Description**

The LX301 is a versatile 1x Active EMI management IC designed to provide system wide reduction of Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) from clock and data sources. The LX301A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The LX30x family of mobile active EMI management ICs is unique in it's design and is based on LFC's proprietary "SaΦic" phase controlled Active EMI

management technology. This allows operation on aperiodic as well periodic signals. By the precise placement of the edges of the reconstructed input signal, the peak energy of the output is distributed over a wider and controlled energy band thereby significantly lowering system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators.

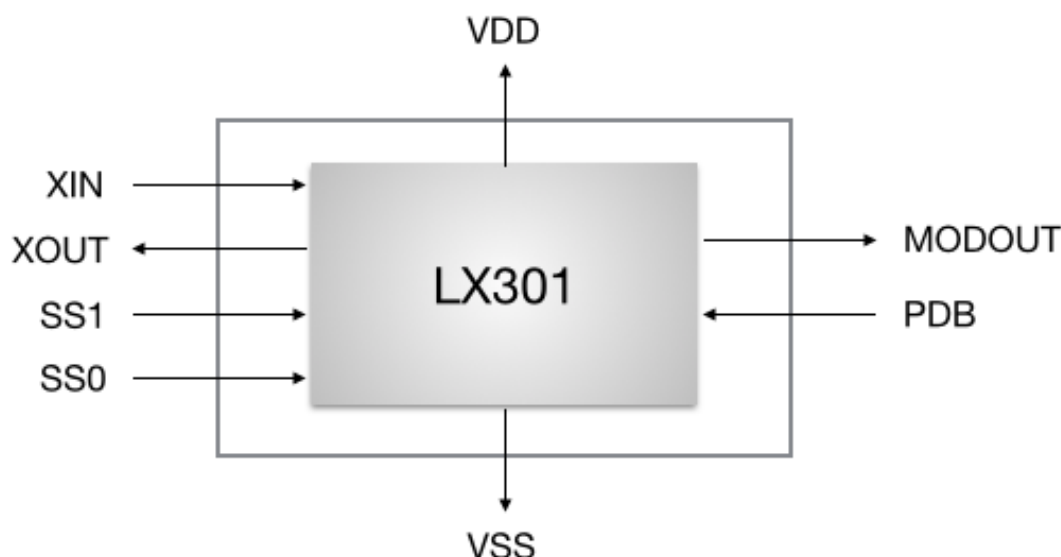
The LX301 has an input frequency range of 1 MHz to 10MHz over a wide voltage range of 1.65V to 3.6V. The device can be placed in a "power save mode" by setting the PDB pin to GND where in it draws typically 0.1uA and also sets the MODOUT pin to a High-Z state. The device has two "deviation control pins" SS1 and SS0 to allow flexibility and optimization of both EMI compliance as well as in system design.

The device is available in an 8 pin DFN package.

**Applications**

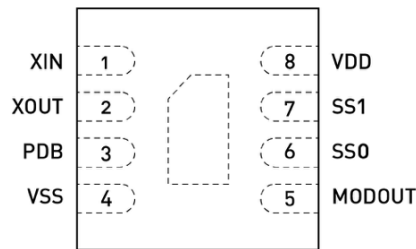
The LX301 is targeted towards mobile platforms such as cell phones, MIDs, Netbooks and other "power and space" sensitive applications.

**Block Diagram**



1.65V – 3.6V, 1x Ultra Low Power Mobile EMI Reduction IC

### Pin Configuration



### Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLKIN	I	Crystal Oscillator Input or Single Ended Clock Input
2	XOUT	O	Crystal Oscillator Output
3	PDB	I	Power Down pin. Active Low. Forces MODOUT to High-Z
4	VSS	P	System ground reference input.
5	MODOUT	O	1X phase modulated buffered output.
6	SS0	I	Deviation Control Pin (refer Functionality Table) Internal Pull-Up Resistor. Recommend external Pull-Down Resistor 0Ω
7	SS1	I	Deviation Control Pin (refer Functionality Table) Internal Pull-Down Resistor. Recommend external Pull-Up Resistor 0Ω
8	VDD	O	System Power Supply pin

### Operating Conditions

Parameter	Description	Min	Max	Unit
V <sub>DD(3.3V)</sub>	Supply Voltage	1.65	3.6	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	-40	+125	°C
C <sub>L</sub>	Load Capacitance		20	pF
C <sub>IN</sub>	Input Capacitance		5	pF

### Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
V <sub>in</sub>	Voltage on any pin with respect to Ground	-0.5 to +4.6	V
T <sub>STG</sub>	Storage temperature	-65 to +125	°C
T <sub>s</sub>	Max. Soldering Temperature (10 sec)	260	°C
T <sub>J</sub>	Junction Temperature	150	°C
T <sub>DV</sub>	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied nor guaranteed for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

## 1.65V – 3.6V, 1x Ultra Low Power Mobile EMI Reduction IC

**Functional Table**

Vdd(V)	Freq. Range (MHz)	Freq. (MHz)	Deviation (%)							
			SS1	SS0	SS1	SS0	SS1	SS0	SS1	SS0
			0	0	0	1	1	0	1	1
1.8	1~10	4	±0.10		±0.20		±0.29		±0.39	
1.8		8	±0.14		±0.31		±0.48		±0.62	
3.3	1~10	4	±0.06		±0.12		±0.19		±0.25	
3.3		8	±0.10		±0.20		±0.29		±0.38	

Note: Specified at V<sub>DD</sub> 1.8V/3.3V and room temperature. Frequency deviation can vary over voltage and temperature by +/-20%

**DC Electrical Characteristics (3.3V +/-0.3V)**

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply Voltage		3.0	3.3	3.6	V
V <sub>IH</sub>	Input HIGH Voltage		0.66*V <sub>DD</sub>			V
V <sub>IL</sub>	Input LOW Voltage				0.33*V <sub>DD</sub>	V
I <sub>IH</sub>	Input HIGH Current (pins 3/6 /7)	V <sub>IN</sub> = V <sub>DD</sub>			10	μA
I <sub>IL</sub>	Input LOW Current (pins 3/6 /7)	V <sub>IN</sub> = 0V			10	μA
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -8mA	0.75*V <sub>DD</sub>			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = +8mA			0.25*V <sub>DD</sub>	V
I <sub>CC</sub>	Static Supply Current	PDB = V <sub>SS</sub>		0.1	1.0	μA
I <sub>DD</sub>	Dynamic Supply Current	4 MHz	Unloaded	1.1	1.7	mA
			10 pF load	1.4	2.0	
Z <sub>o</sub>	Output Impedance			25		Ω

**Switching Characteristics (3.3V +/-0.3V)**

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		1	5	10	MHz
MODOUT	Output Frequency		1	5	10	
$T_d$	Duty Cycle <sup>1,2</sup> = $(t_2 / t_1) * 100$	Measured at $V_{DD} / 2$	45	50	55	%
$t_3$	Output Rise Time <sup>1,2</sup>	Measured between 20% to 80%	1.0	1.5	2.0	nS
$t_4$	Output Fall Time <sup>1,2</sup>	Measured between 80% to 20%	1.0	1.5	2.0	nS
$t_j$	Cycle-to-cycle jitter <sup>2</sup>	Unloaded outputs 4 MHz		+/-250		pS

**Notes:**

1. All parameters specified with 4MHz without loaded outputs and  $V_{DD}$  3.3V.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

**DC Electrical Characteristics 1.8V +/-0.15V)**

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
$V_{DD}$	Supply Voltage		1.65	1.8	1.95	V
$V_{IH}$	Input HIGH Voltage		0.66*Vdd			V
$V_{IL}$	Input LOW Voltage				0.33*Vdd	V
$I_{IH}$	Input HIGH Current (pins 6 and 7)	$V_{IN} = V_{DD}$			10	$\mu$ A
$I_{IL}$	Input LOW Current (pins 6 and 7)	$V_{IN} = 0V$			10	$\mu$ A
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -4mA$	0.75*Vdd			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = +4mA$			0.25*Vdd	V
$I_{CC}$	Static Supply Current	PDB = VSS		0.1	1.0	$\mu$ A
$I_{DD}$	Dynamic Supply Current	4 MHz	Unloaded	0.6	0.9	mA
			10 pF load	0.7	1.0	
$Z_o$	Output Impedance			25		$\Omega$

**Switching Characteristics (1.8V +/-0.15V)**

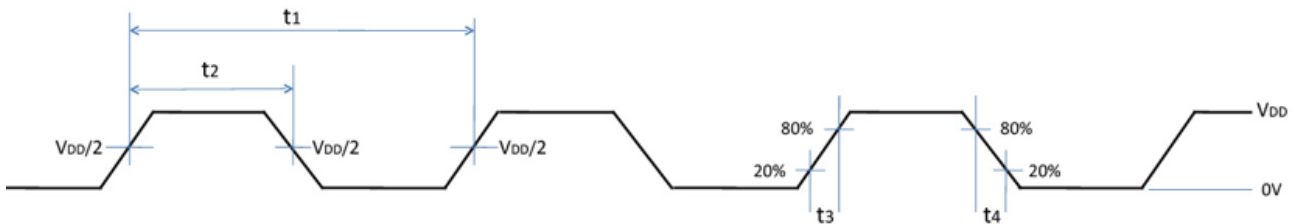
Parameter	Description	Test Conditions	Min	Typ	Max	Unit
INPUT	Input Frequency		1	4	10	MHz
MODOUT	Output Frequency		1	4	10	
$T_d$	Duty Cycle $^{1,2} = (t_2 / t_1) * 100$	Measured at $V_{DD} / 2$	45	50	55	%
$t_3$	Output Rise Time $^{1,2}$	Measured between 20% to 80%	1.0	2.0	3.5	nS
$t_4$	Output Fall Time $^{1,2}$	Measured between 80% to 20%	1.0	2.0	3.5	nS
$t_j$	Cycle-to-cycle jitter $^2$	Unloaded outputs 4 MHz		+/-250		pS

Notes:

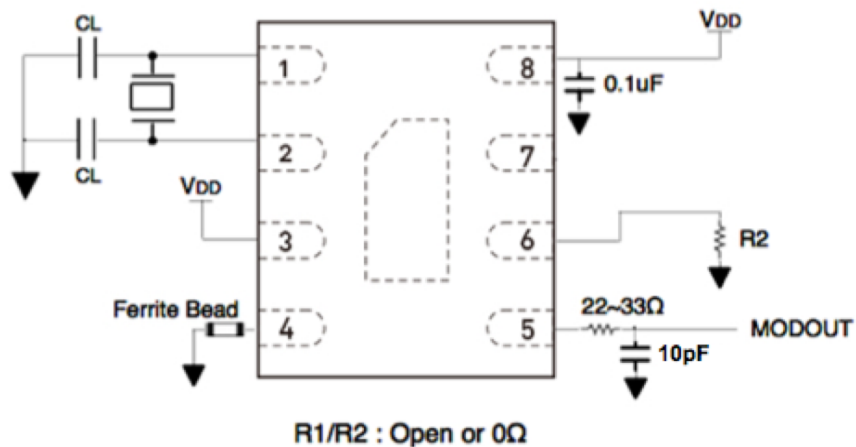
1. All parameters specified with 4MHz without loaded outputs and  $V_{DD}$  1.8V.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

**Duty Cycle Timing**

**All Outputs Rise/Fall Time**

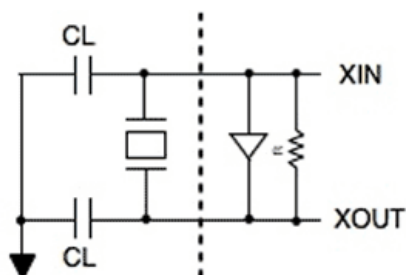


**Application Schematic**



**1.65V – 3.6V, 1x Ultra Low Power Mobile EMI Reduction IC**

### Crystal Oscillator Circuit

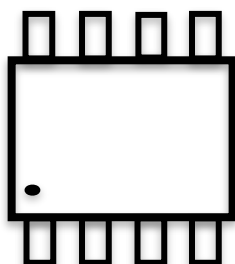


$$CL = 2 \times (C_p - C_s)$$

Cp: load capacitance of Crystal

Cs: Stray capacitance ( PCB trace + Input cap. of IC )

### Marking Information



**XXX**: Part Number

**T**: Temperature Grade

**Y**: Year of Production

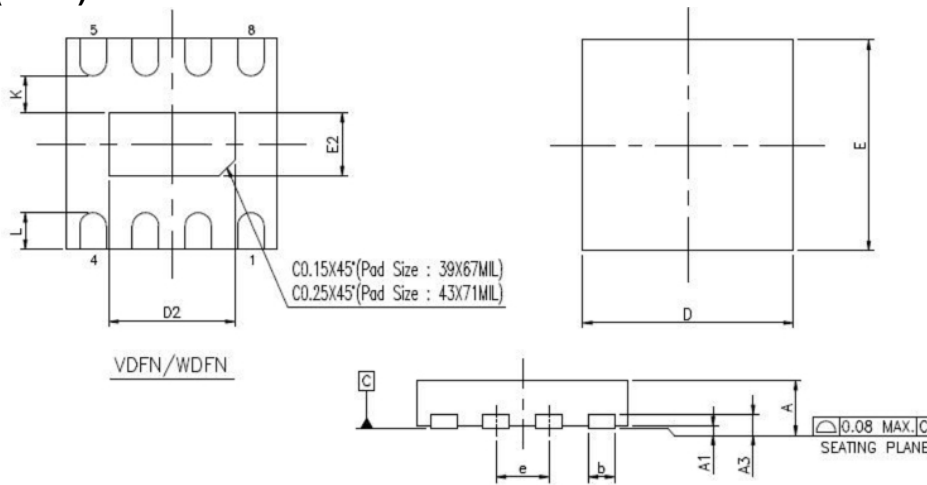
**WWW**: Work Order No.

### Ordering Information

Part Number	Temp. Grade Indicator	Temp Grade	Temp Range	IC Marking	IC Package	Tape & Reel
LX301C	C	Commercial	0°~70°C	301C	2mm x 2mm 8L WDFN	4,000 pcs / Reel
LX301I	I	Industrial	-20°~85°C	301I		
LX301E	E	Automotive AEC Q100 Grade 2	-40°~105°C	301E		
LX301A	A	Automotive AEC Q100 Grade 1	-40°~125°C	301A		

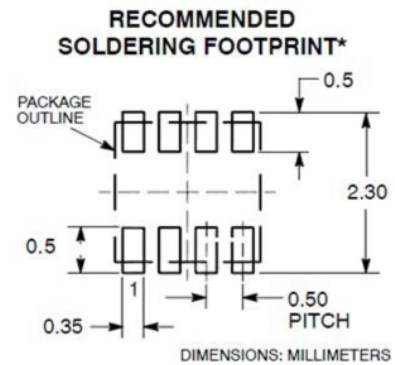
## 1.65V – 3.6V, 1x Ultra Low Power Mobile EMI Reduction IC

**Package Dimension  
WDFN(X208)**



JEDEC OUTLINE	MO-229		
PKG CODE	WDFN (X208)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	.5 BSC		
K	0.20	---	---

- NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
  3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.



PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	VDFN	WDFN	UDFN (OPEN)	TDFN (OPEN 2)
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Sn	PPF					
39X67*	1.15	1.20	1.25	0.60	0.65	0.70	0.20	0.35	0.45	V	X	N/A	V	V	---	---

\*表示汎用字元, 此汎用字元可能被其它不同字元所取代, 實際的字元請參照bonding diagram所示。  
\* is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

**Revision History**

Revision Number	Date of Release	Changes
1.1	3/12/2019	1) Input frequency range change 2) Deviation Update
1.2	7/30/2020	1) Update AC/DC characteristics 2) Ordering information updates

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Notice: The information in this document is subject to change without notice.